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April 26, 2000

Box Patent Application

BY HAND DELIVERY

Assistant Commissioner for Patents
Washington, D.C. 20231

Re: Non-Provisional Utility Patent Application
Application No.: To be Assigned; Filed: April 26, 2000
For: **Thin Film Transistor Array Panel and Methods for Manufacturing the Same**
Inventors: **Dong-Gyu KIM; and Jong-Soo YOON**
Our Ref: 06192.0132

Sir:

The following documents are forwarded herewith for appropriate action by the U.S. Patent and Trademark Office:

1. Utility Patent Application Transmittal Form;

2. Fee Transmittal Form 1082 (duplicate); and

3. U.S. Utility Patent Application entitled:

Thin Film Transistor Array Panels and Methods for Manufacturing the Same

and naming as inventors:

Dong-Gyu KIM; and Jong-Soo YOON

the application consisting of:

a. a specification containing:

(i) **27** pages of description prior to the claims;
(ii) **14** pages of claims (**63** claims); and
(iii) a one (1) page abstract;

b. 41 sheets of drawings: (Figs. 1-3, 4A-4C, 5A-5B, 6A-6C, 7A-7C, 8A-8C, 9A-9C, 10A-10B, 11A-11B, 12A-12B, 13A-13C, 14-16, 17A-17C, 18A-18C, 19A-19B, 20A-20C, 21-23, inclusive);

4. Our check no. 327134 for $1,738.00 to cover:

   $1,698.00 filing fee for patent application;
   $ 40.00 recordation assignment filing fee

5. A copy of Combined Declaration and Power of Attorney for Patent Application;

6. Form PTO-1595 Recordation Cover Sheet and a copy of the executed Assignment to Samsung Electronics Co., Ltd., recordation of which is hereby respectfully requested; and

7. Two (2) return postcards.

It is respectfully requested that, of the two attached postcards, one be stamped with the filing date of these documents and returned to our courier, and the other, prepaid postcard, be stamped with the filing date and unofficial application number and returned as soon as possible.

Applicant hereby claims foreign priority benefits under Title 35, United States Code, § 119 to Korean Application Nos. 1999-14896, 1999-14898 and 2000-19712 respectively filed April 26, 1999, April 26, 1999 and April 14, 2000.

The U.S. Patent and Trademark Office is hereby authorized to charge any fee deficiency, or credit any overpayment, to our Deposit Account No. 08-3038. A duplicate copy of this letter is enclosed.

Respectfully submitted,

Michael J. Bell
Registration No. 39,604

Enclosures

Please type a plus sign (+) inside this box → [+]

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UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b))

Attorney Docket No.	06192.0132
First Named Inventor or Application Identifier	Dong-Gyu KIM et al.
Title	Thin Film Transistor Array Panel and Methods for Manufacturing the Same
Express Mail Label No.	

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents

ADDRESS TO: Assistant Commissioner for Patents
Box Patent Application
Washington, DC 20231

1. [X] *Fee Transmittal Form (Form PTO-1082)
(Submit an original and a duplicate for fee processing)
2. [X] Specification [*Total Pages* 42]
(preferred arrangement set forth below)
- Descriptive title of the Invention
- Cross References to Related Applications
- Statement Regarding Fed sponsored R&D
- Reference to Microfiche Appendix
- Background of the Invention
- Brief Summary of the Invention
- Brief Description of the Drawings (if filed)
- Detailed Description
- Claims
- Abstract of the Disclosure
3. [X] Drawing(s) *(35 USC 113)* [*Total Sheets* 41]
4. Oath or Declaration [*Total Pages* 3]
   a. [X] Newly executed (original or copy)
   b. [ ] Copy from a prior application (37 CFR 1.63(d))
   (for continuation/divisional with Box 17 completed)
   [Note Box 5 below]
   i. [ ] DELETION OF INVENTOR(S)
   Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).
5. [ ] Incorporation By Reference *(useable if Box 4b is checked)*
The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.
6. [ ] Microfiche Computer Program *(Appendix)*
7. Nucleotide and/or Amino Acid Sequence Submission
(if applicable, all necessary)
   a. [ ] Computer Readable Copy
   b. [ ] Paper Copy (identical to computer copy)
   c. [ ] Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. [X] Assignment Papers (cover sheet & document(s))
9. [ ] 37 CFR 3.73(b) Statement *(when there is an assignee)* [ ] Power of Attorney
10. [ ] English Translation Document *(if applicable)*
11. [ ] Information Disclosure Statement (IDS)/PTO-1449 [ ] Copies of IDS Citations
12. [ ] Preliminary Amendment
13. [X] Return Receipt Postcard (MPEP 503) (Two)
(should be specifically itemized)
14. [ ] *Small Entity Statement(s) [ ] Statement filed in prior application, Status still proper and desired
15. [X] Certified Copy of Priority Document(s)
(if foreign priority is claimed)
16. [ ] Other:

*NOTE FOR ITEMS 1 & 14 IN ORDER TO BE ENTITLED TO PAY SMALL ENTITY FEES, A SMALL ENTITY STATEMENT IS REQUIRED (37 C F R § 1 27), EXCEPT IF ONE FILED IN A PRIOR APPLICATION IS RELIED UPON (37 C F R. § 1 28)

17. **If a CONTINUING APPLICATION**, *check appropriate box and supply the requisite information:*
[ ] Continuation [ ] Divisional [ ] Continuation-in-part (CIP) of prior application No: /
Prior Application Information: Examiner: Group/Art Unit:

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PATENT TRADEMARK OFFICE

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Name (Print/Type)	Michael J. Bell	*Registration No. (Attorney/Agent)*	39,604
Signature		*Date*	April 26, 2000

Burden Hour Statement This form is estimated to take 0 2 hours to complete Time will vary depending upon the needs of the individual case Any comments on the amount of time you are required to complete this form should be sent to the Chief Information Officer, Patent and Trademark Office, Washington, DC 20231 DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS SEND TO Assistant Commissioner for Patents, Box Patent Application, Washington, DC 20231

FORM PTO-1082

HOWREY SIMON ARNOLD & WHITE, LLP
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Attorney Docket No. 0 6192.0132

ASSISTANT COMMISSIONER FOR PATENTS
Washington, D.C. 20231

Sir:

Transmitted herewith for filing is the patent application of
Inventor(s): **Dong-Gyu KIM; and Jong-Soo YOON**
For: **THIN FILM TRANSISTOR ARRAY PANEL AND METHODS FOR MANUFACTURING THE SAME**

Enclosed are:

x 41 sheets of drawings. (Figs. 1-3, 4A-4C, 5A-5B, 6A-6C, 7A-7C, 8A-8C, 9A-9C, 10A-10B, 11A-11B, 12A-12B, 13A-13C, 14-16, 17A-17C, 18A-18C, 19A-19B, 20A-20C, 21-23, inclusive)
x An assignment of the invention to SAMSUNG ELECTRONICS CO., LTD.
x Form PTO-1595.
___ A certified copy of Korean Priority Document Patent Application No. 99-54873
___ An associate power of attorney.
___ A verified statement to establish small entity status under 37 CFR 1.9 and 37 CFR 1.27.
___ Executed Power of Attorney from Assignee.
x Executed Declaration for Patent Application.

The filing fee has been calculated as shown below:

	(Col. 1)	(Col. 2)	SMALL ENTITY			OTHER THAN A SMALL ENTITY	
FOR	NO. FILED	NO. EXTRA	RATE	FEE	OR	RATE	FEE
BASIC FEE				$ 380.00	OR		$690.00
TOTAL CLAIMS	63 -20 =	* 43	x 9 =		OR	43 x 18 =	774.00
INDEP. CLAIMS	6 -3 =	* 3	x 39 =		OR	3 x 78 =	234.00
☐ MULTIPLE DEPENDENT CLAIM PRESENTED			+ 130 =		OR	+ 260 =	
*If the difference in Col. 1 is less than zero, enter "0" in Col. 2			TOTAL		OR	TOTAL	$1,698.00

_ Please charge my Deposit Account No. 08-3038 in the amount of _____. A duplicate copy of this sheet is attached.

xx A check in the amount of $1,738.00 to cover the filing fees and the assignment recordation fee is enclosed.

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_ Any patent application processing fees under 37 CFR 1.17
_ The issue fee set in 37 CFR 1.18 at or before mailing of the Notice of Allowance, pursuant to 37 CFR 1.311(b).
_ Any filing fees under 37 CFR 1.16 for presentation of extra claims.

Date April 26, 2000

Michael J. Bell (Reg. No. 39,604)

THIN FILM TRANSISTOR ARRAY PANEL AND METHODS FOR MANUFACTURING THE SAME

BACKGROUND OF THE INVENTION

(a) Field of the Invention

The present invention relates to thin film transistor array panels and the manufacturing methods of the same.

(b) Description of the Related Art

A liquid crystal display (LCD) is one of the most popular flat panel display (FPD). The liquid crystal display has two panels having electrodes for generating electric fields and a liquid crystal layer interposed therebetween.

The transmittance of incident light is controlled by the intensity of the electric field applied to the liquid crystal layer.

In the most widely used liquid crystal display, the field-generating electrodes are provided at both of the panels, with one of the panels having switching elements such as thin film transistors, and the other panel having color filters.

In general, a thin film transistor array panel is manufactured by a photolithography process using five or six photomasks and a color filter panel is manufactured by a photolithography process using three or four photomasks.

Since the photolithography process costs expensive, the number of the photolithography steps needs to be minimized.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to pr

manufacturing thin film transistor array panels for liquid cr

reduced number of masks employed in the photolithography processes.

It is another object of the present invention to simplify methods for manufacturing thin film transistor array panels for liquid crystal displays.

These and other objects are provided, according to the present invention, by forming a portion of a photoresist layer (photoresist) that is thinner than another portion between a source electrode and a drain electrode before the two electrodes are formed. Thus, the thin portion protects underlayers when some layers are etched, and is also etched along with other layers to expose its underlayer. Also, red, green, and blue color filters are used as a passivation layer covering a thin film transistor and wires. A wire may be formed of a photosensitive conductive material. The color filters may be formed of photosensitive material and screen printed or offset printed. A light blocking layer made of the color filter may be formed on the channel of the thin film transistor.

In a manufacturing method according to the present invention, a gate wire including a gate line and a gate electrode connected to the gate line is formed on an insulating substrate. A gate insulating layer pattern covering the gate wire, a semiconductor pattern, and an ohmic contact layer pattern are formed. A data wire including a data line, a source electrode and a drain electrode is formed. The source electrode and the drain electrode are made of the same layer on the ohmic contact layer and separated from each other. The data line is connected to the source electrode. Then, red, green, and blue color filters covering the data wire is formed. The color filter has a first contact hole exposing the drain electrode. A pixel electrode is formed and connected to the drain electrode through the first contact hole. Here, the source electrode and the drain electrode are separated by a

photolithography process using a photoresist pattern, and the photoresist pattern has a first portion having a first thickness that is at least located between the source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

It is preferable that a mask used for forming the photoresist pattern has a first, a second, and a third part, and that the transmittance of the third part is higher than the first and the second parts, the transmittance of the first part is higher than the second part, the photoresist pattern is made of positive photoresist, and the mask is aligned such that the first, the second, and the third parts respectively face the first, the second, and the third portions of the photoresist pattern in an exposing step.

The first part of the mask may include a partially transparent layer, or a pattern smaller than the resolution of the exposure used in the exposing step.

BRIEF DESCRIPTION OF THE DRAWINGS

The accompanying drawings, which are incorporated in and constitute a part of the specification, illustrate an embodiment of the invention, and, together with the description, serve to explain the principle of the invention.

FIG. 1 is a layout view of a thin film transistor array panel for a liquid crystal display according to the first embodiment of the present invention.

FIGs. 2 and 3 are cross-sectional views taken along lines II-II' and III-III' of FIG. 1, respectively.

FIG. 4A is a layout view of the thin film transistor array panel according to the first embodiment of the present invention showing a first manufacturing step.

FIGs. 4B and 4C are cross-sectional views taken along the lines IVB-IVB' and IVC-IVC' of FIG. 4A.

FIGs. 5A and 5B are cross-sectional views at the next step following FIGs. 4B and 4C taken along the lines IVB-IVB' and IVC-IVC' of FIG. 4A.

FIG. 6A is a layout view of thin film transistor array panel at the next step following FIGs. 5A and 5B.

FIGs. 6B and 6C are respectively cross-sectional views taken along the lines VIB-VIB' and VIC-VIC' of FIG. 6A.

FIGs. 7A, 7B, and 7C, FIGs. 8A, 8B, and 8C, and FIGs. 9A, 9B, and 9C are embodiments of a photoresist layer having various thicknesses.

FIGs. 10A, 11A, and 12A are cross-sectional views at the next step following FIGs. 6B taken along the line VIB-VIB' of FIG. 6A.

FIGs. 10B, 11B, and 12B are cross-sectional views at the next step following FIG. 6C taken along the line VIC-VIC' of FIG. 6A.

FIG. 13A is a layout view of thin film transistor array panel at the next step following in FIGs. 12A and 12B.

FIGs. 13B and 13C are the cross-sectional views taken along the lines XIIIB-XIIIB' and XIIIC-XIIIC' of FIG. 13A, respectively.

FIG. 14 is a layout view of a thin film transistor array panel for a liquid crystal display according to the second embodiment of the present invention.

FIGs. 15 and 16 are cross-sectional views taken along lines XV-XV' and XVI-XVI' of FIG. 14, respectively.

FIG. 17A is a layout view of the thin film transistor array panel according to the second embodiment of the present invention showing a first manufacturing step.

FIGs. 17B and 17C are cross-sectional views taken along the lines XVIIB-XVIIB' and XVIIC-XVIIC' of FIG. 17A.

FIG. 18A is a layout view of the thin film transistor array panel in the next step following FIGs. 17A.

FIGs. 18B and 18C are respectively cross-sectional views taken along the lines XVIIIB-XVIIIB' and XVIIIC-XVIIIC' of FIG. 18A.

FIGs. 19A and 19B are cross-sectional views at the next step following FIGs. 18B and 18C taken along the lines XVIIIB-XVIIIB' and XVIIIC-XVIIIC' of FIG. 18A.

FIG. 20A is a layout view of thin film transistor array panel in the next step following in FIGs. 19A and 19B.

FIGs. 20B and 20C are the cross-sectional views taken along the lines XXB-XXB' and XXC-XXC' of FIG. 20A, respectively.

FIG. 21 is a layout view of a thin film transistor array panel for a liquid crystal display according to the third embodiment of the present invention.

FIGs. 22 and 23 are cross-sectional views taken along lines XXII-XXII' and XXIII-XXIII' of FIG. 21, respectively.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

The present invention now will be described more fully hereinafter with reference to the accompanying drawings, in which preferred embodiments of the invention are shown. This invention may, however, be embodied in many different forms and should not be construed as limited to the embodiments set forth herein. In the drawings, the thickness of layers and regions are exaggerated for clarity. Like numerals refer to like elements throughout. It will be understood that when an

element such as a layer, region, or substrate is referred to as being "on" another element, it can be directly on the other element or intervening elements may also be present. In contrast, when an element is referred to as being "directly on" another element, there are no intervening elements present.

The number of manufacturing steps are reduced with the manufacturing method of the present invention by forming a photoresist pattern having a thinner portion between electrodes in the step of separating a source electrode from a drain electrode of the same layer, and by converting a passivation layer to red, green, and blue color filters.

FIG. 1 is a layout view of a thin film transistor array panel for a liquid crystal display according to the first embodiment of the present invention, and FIGs. 2 and 3 are the cross-sectional views taken along lines II-II' and III-III' of FIG. 1.

Gate wires of metal or conductive material such as aluminum (Al) or aluminum alloy, molybdenum (Mo) or molybdenum-tungsten (MoW), chromium (Cr), and tantalum (Ta) are formed on an insulating substrate 10. A gate wire includes a gate line (or scanning signal line) 22 extending in the horizontal direction in FIG. 1, a gate pad 24 connected to an end of the gate line 22 and transmitting a scanning signal from an external circuit to the gate line 22, a gate electrode 26 that is a part of the thin film transistor, and a storage electrode 28 that is parallel with the gate line 22 and receives a voltage such as a common voltage applied to a common electrode (not shown) on an upper panel of the liquid crystal display. The storage electrode 28 provides the storage capacitance along with a conductor pattern 68 connected to a pixel electrode 82 that will be described later. The liquid crystal capacitor includes the pixel electrode 82 and the common electrode. The storage electrode 28 may not

be necessary if the storage capacitance between the pixel electrode 82 and the gate line 22 is sufficient.

The gate wire parts 22, 24, 26, and 28 may have either a multiple-layered structure or a single-layered structure. When the gate wire parts 22, 24, 26, and 28 form a multiple-layered structure, it is preferable that one layer is made of a material having a low resistivity and another layer is made of a material having good contacting properties with other materials. Double layers of Cr/Al (or Al alloy) and Al/Mo are examples.

Gate insulating layers 32 and 38 of silicon-nitride (SiNx) are formed on the gate wire parts 22, 24, 26, and 28, and the insulating substrate 10. The gate insulating layer pattern 32 covers the gate electrode 26.

Semiconductor patterns 42 and 48 (made of semiconductor such as hydrogenated amorphous silicon) are formed on the gate insulating layer 32 and 34. Ohmic contact layer patterns 55, 56, and 58 (made of such materials as amorphous silicon heavily doped with impurities like phosphorus) are formed on the semiconductor patterns 42 and 48.

A data wire made of conductive materials such as Mo or MoW, Cr, Al or Al alloy, and Ta is formed on the ohmic contact layer patterns 55, 56, and 58. The data wire has a data line part including a data line 62 extending in the vertical direction on FIG. 1, a data pad 64 connected to an end of data line 62 and transmitting image signals from an external circuit to the data line 62 and a source electrode 65 of a thin film transistor connected to data line 62. The data wire also includes a drain electrode 66 of the thin film transistor on the other side of the gate electrode 26 or the channel part C of a thin film transistor and is separated from the data line parts

62, 64, 65, and conductor pattern 68 used for storage capacitance located on the storage electrode 28. When the storage electrode 28 is not provided, the conductor pattern 68 is not necessary.

The data wire parts 62, 64, 65, 66, and 68 may have a multiple-layered structure like the gate wire parts 22, 24, 26, and 28. Of course, when the data wire has a multiple-layered structure, it is preferable that one layer is made of a material having a low resistivity and another is made of a material having good contacting properties.

The ohmic contact layer patterns 55, 56, and 58 reduce the contact resistance between the semiconductor patterns 42 and 48 and the corresponding data wire parts 62, 64, 65, 66, and 68, and have the same layout as the data wire parts 62, 64, 65, 66, and 68. In other words, a first ohmic contact layer portion 55 under the data line part has the same shape as the data line parts 62, 64, and 65, a second ohmic contact layer portion 56 under the drain electrode part has the same shape as the drain electrode 66, and a third ohmic contact layer portion 58 under the conductor pattern 68 has the same shape as the conductor pattern 68 for the storage capacitor. Here, the ohmic contact layer patterns 55, 56, and 58 may be extended out from the data wire parts 62, 64, 65, 66, and 68.

The semiconductor patterns 42 and 48 have the same layout as the corresponding data wire parts 62, 64, 65, 66, and 68 and the corresponding ohmic contact layer patterns 55, 56, and 58 except for the channel part C of the thin film transistor. Or, more concretely, the semiconductor portion 42, the conductor pattern 68, and the third ohmic contact layer portion 58 all have the same shape, but the semiconductor portion 42 has a shape different from the data wire and the ohmic

contact layer pattern. In other words, the data line parts 62, 64, and 65, especially the source electrode 65 and the drain electrode 66, are separated from each other by the channel part C of the thin film transistor and the portions 55 and 56 of the underlying ohmic contact layer pattern are also separated from each other. But the semiconductor portion 42 is not divided into two pieces so that it traverses the channel of a thin film transistor.

Red, blue and green color filters 75, 77, and 79 are formed on the data wire parts 62, 64, 65, 66, and 68, the gate wire parts 22, 24, 26, and 28, and the substrate 10 which is not covered by the data wire parts 62, 64, 65, 66, and 68. The color filters 75, 77, 79 have contact holes 71, 72, 73, and 74 respectively exposing the drain electrode 66, the gate pad 24, the data pad 64, and the conductor pattern 68 provided for storage capacitance.

Pixel electrodes 82 that receive an image signal and generate an electric field with a common electrode of an upper panel are formed on the color filters 75, 77, and 79. The pixel electrode 82 is made of a transparent conductive material such as indium tin oxide (ITO). The pixel electrode 82 is connected to the drain electrode 66 both physically and electrically through the contact hole 71, and receives the image signal from the drain electrode. Even though the aperture ratio is increased when the pixel electrode 82 overlaps the gate lines 22 or the adjacent the data lines, these lines are not required to overlap the pixel electrode. The pixel electrode 82 is connected to the conductor pattern 68 for storage capacitance through the contact hole 74 and transmits an image signal to the conductor pattern 68.

A redundant gate pad 84 and a redundant data pad 86 respectively connected to the gate pad 24 and the data pad 64 through the contact holes 72 and 73 are

formed on the gate pad 24 and the data pad 64. These redundant pads 84 and 86 are optional as they protect the pads 24 and 64 from corrosion by the ambient air and strengthen the adhesion between the external circuit and the pads 24 and 64.

A method for manufacturing a thin film transistor array panel according to an embodiment of the present invention will now be described with reference to the FIGS. 4A to 13C and FIGS. 1 to 3.

At first, as shown in FIGs. 4A to 4C, a layer of conductor, such as a metal, is deposited on a substrate 10 by such methods as sputtering to a thickness of 1,000 Å to 3, 000 Å, and gate wire parts including a gate line 22, a gate pad 24, a gate electrode 26, and a storage electrode 28 are formed by dry or wet etching using a first mask.

Next, as shown in FIGs. 5A and 5B, a gate insulating layer 30, a semiconductor layer 40, and an ohmic contact layer 50 are sequentially deposited to thicknesses of 1,500 Å to 5,000 Å, 500 Å to 2,000 Å, and 300 Å to 600 Å, respectively, by such methods as chemical vapor deposition (CVD). Then, a conductor layer 60, such as a metal, is deposited to a thickness of 1,500 Å to 3,000 Å by such methods as sputtering and a photoresist layer 110 having a thickness of 1 μ to 2 μ is coated on the conductive layer 60.

Thereafter, the photoresist layer 110 is exposed to light through a second mask and developed to form photoresist patterns 112 and 114 as shown in FIGs. 6B and 6C. At this time, the first portion 114 of the photoresist pattern located between a source electrode 65 and a drain electrode 66, i.e., a thin film transistor channel part C as shown in FIG. 6C, is thinner than the second portion 112 of photoresist pattern located over the data wire portion A where a data wire parts 62, 64, 65, 66, and 68

will be formed. Additionally, the third portion, or the remaining portion of the photoresist pattern located at portion B, is thinner than the first portion. The third portion may have a thickness that varies according to the etching method. For example, the third portion has a substantially zero thickness when using a wet etch, but the third portion may have a non-zero thickness when using a dry etch. At this time, the thickness ratio between the first portion 114 and the second portion 112 depends on the etch conditions that will be described later. However, it is preferable that the thickness of the first portion 114 is equal to or less than half of the second portion 112, or for example, less than 4,000 Å. More preferably, the thicknesses of the second portion and the first portion are respectively 16,000-19,000 Å and about 3,000 Å.

There are many methods that can make the thickness of the photoresist layer different depending on the position, and two methods using positive photoresist will be described.

The first method, as shown in FIGs. 7A to 7C, is controlling the amount of incident light by forming a pattern such as a slit or a lattice that is smaller than the resolution of the exposure device, or by providing a partly-transparent layer on the mask.

At first, as shown in FIG. 7A, a photoresist layer 200 is coated on a thin film 300 on a substrate. At this time, it is preferable that the photoresist layer 200 is thicker than normal to control the thickness of the photoresist layer after development.

Next, as shown in FIG. 7B, light is illuminated on the photoresist layer 200 through a photomask 400 having a plurality of slits 410. At this time, the size of the

slit 410 and the opaque portion 420 between the slits are smaller than the resolution of the exposure device. When a partly-transparent layer is used, a Cr layer of some thickness (not shown) is left on the mask 400, thereby reducing the amount of exposing light. Alternatively, a mask including films of different transmittances may be used.

When the photoresist layer 200 is exposed to light, the polymers of the photoresist layer 200 are disintegrated by the light. As the amount of the light increases, the polymers may even be completely disintegrated. The exposure step is finished when the polymers of a portion that is directly exposed to the light, for example, the left and right ends of the polymers in FIG. 7B, are completely disintegrated. However, the polymers of the photoresist layer 200 portion that are exposed through the slit pattern 410 are not completely disintegrated because the amount of incident light is less than that of the directly exposed portion. If the exposure time is too long, all the polymers of the photoresist layer 200 are disintegrated. Therefore, this should be avoided. In FIG. 7B, the reference numeral 210 indicates the removed part and the reference numeral 220 indicates the still remaining part.

Only the part 220 is left after developing the photoresist layers 210 and 220, and a thinner portion is left at the center that was exposed to light less than the fully exposed portion as shown in FIG. 7C.

The second method to make the thickness of the photoresist layer different is reflowing. This is described with reference to the examples shown in the FIGs. 8A to 8C and FIGs. 9A to 9C.

As shown in FIG. 8A, portions 210 and 220 of a photoresist layer are exposed

to light through a mask 400 having respectively substantially transparent portions and substantially opaque portions. The portion 210 is a portion in which all polymers are disintegrated, and the other portion 220 is a portion in which all polymers remain. Then, as shown in FIG. 8B, the photoresist layer is developed to form a photoresist pattern having portions of zero and nonzero thicknesseses. However, as described above, the portion with zero thickness may have some residual thickness of photoresist. The photoresist pattern is subject to reflow such that the photoresist 220 flows into the zero thickness portions to form a new photoresist pattern 250.

However, the zero thickness portions between the photoresist portions 220 may not be completely covered with photoresist by reflowing. To avoid such a case, an opaque pattern 430, which is smaller than the resolution of the exposure device, is provided on the mask 400 as shown in FIG. 9A. Then, as shown in FIG. 9B, a thinner portion 230 is formed between the thick portions 220 after development. By reflowing this photoresist pattern, a photoresist pattern 240 having a thick portion and a thin portion between the thick portions is formed.

Using these methods, a photoresist pattern having different thickness at different positions is obtained.

Referring back to FIG. 6C, the photoresist pattern 114 and the underlying layers including the conductor layer 60, the ohmic contact layer 50, the semiconductor layer 40, and the gate insulating layer 30 are subject to an etching process. After this step, a data wire and the underlying layers at the data wire part A and the semiconductor layer on the channel part C are left. Four layers of 60, 50, 40, and 30 in the remaining part B are removed from the substrate 10.

As shown in FIGs. 10A and 10B, the ohmic contact layer 50 of the part B is

exposed by removing the conductor layer 60 thereon. At this time, both wet etch and dry etch can be used, and it is preferable that the conductor layer 60 is etched but the photoresist layers 112 and 114 are not etched. However, a dry etch method cannot meet such a condition. Therefore, when a dry etch method is employed, the first portion 114 needs to be made thicker than in the wet etch case so that the conductor layer 60 is not exposed.

If the conductor layer 60 is made of Mo or MoW alloy, Al or Al alloy, or Ta, either dry etch method or wet etch methods can be used. However, if the conductor layer 60 is made of Cr, a wet etch is better because Cr is not easily removed by dry etch. $CeNHO_3$ is available as a wet etchant for etching a Cr conductor layer 60. A gas mixture of CF_4 and HCl or CF_4 and O_2 is used for dry etching a Mo or MoW conductor layer 60. The etch rate of the mixture of CF_4 and O_2 system on the photoresist layer is similar to that of the conductor layer 60.

As shown in FIGs. 10A and 10B, only the portions of the conductor 60 under the photoresist layers 112 and 114 at the channel part C and the data wire part B for source/drain electrodes and a storage capacitor are left. The remaining portion of the conductor layer 60 at part B is totally removed to expose the underlying ohmic contact layer 50. At this time, the conductor patterns 67and 68 have the same layout as the data wire parts 62, 64, 65, 66, and 68 except that the source electrode 65 and the drain electrode 66 are connected. When a dry etch is used, the photoresist layers 112 and 114 are also etched to a certain thickness.

Next, the exposed portions of the ohmic conductor layer 50 at part B, the semiconductor layer 40, and the gate insulating layer 30 thereunder of FIGs. 10A and 10B are removed by dry etching along with first portion 114 of the photoresist

layer, as shown in FIGs. 11A and 11B. The photoresist patterns 112 and 114, the ohmic contact layer 50, the semiconductor layer 40, and the gate insulating layer 30 are all etched (the semiconductor layer and the ohmic contact layer have almost the same etch rate), but the gate wire parts 22, 24, 26, and 28 must not be etched. If the etch rates of the photoresist patterns 112 and 114, the semiconductor layer 40, and the gate insulating layer 30 are almost the same, the thickness of the first portion 114 is equal to or less than that of the sum of the semiconductor layer 40, and the gate insulating layer 30. The portion of the gate insulating layer 30 covering the substrate 30 and the gate wire parts 22, 24, 26, and 28 may remain after etching.

Then, as shown in FIGs. 11A and 11B, the conductor pattern 67 is exposed by removing the first portion 114 of the channel part C, and the substrate 10 and the gate wire part 22, 24, 26, and 28 are exposed by removing the ohmic contact layer 50, the semiconductor layer 40, and the gate insulating layer 30 of the part B shown in FIG 11B. At the same time, the thickness of the second portion 112 over the data wire part A is reduced by etching. Furthermore, the semiconductor patterns 42 and 48, and the gate insulating layers 32 and 38 are completed at this step. The reference numerals 57 and 58 respectively represent the ohmic contact layer pattern under the conductor patterns 67 and 68 for the source/drain electrode and the storage capacitor.

The remaining photoresist layer on the conductor pattern 67 is then removed by ashing or plasma etching.

Next, as shown in 12A and 12B, the conductor pattern 67 for source/drain electrodes at the channel part C and the ohmic contact layer pattern 57 for source/drain electrodes of FIG 11B are removed by etching. At this time, it is

possible either to etch both the conductor pattern 67 and the ohmic contact layer 57 by a dry etching method, or to etch the conductor pattern 67 by a wet etching method and the ohmic contact layer 57 by a dry etching method. In the former case, it is preferable that the etching methods showing a large etch selectivity between the conductor pattern 67 and the ohmic contact layer pattern 57 are employed. If the etch selectivity is not large enough, it is hard to detect the etch stop point and to control the thickness of the semiconductor pattern 42 around the channel part C. A gas mixture of SF_6 and O_2, for example, meets such conditions. In the latter case of doing the wet etch and the dry etch sequentially, the lateral sides of the conductor pattern 67 subject to wet etch are also etched, while those of the ohmic contact layer pattern 57, which is dry etched, are hardly etched at all. Thereby, the profile of these two patterns 67 and 57 makes a step like form. The gas mixture of CF_4 and O_2 is an example of an etch gas system for etching the ohmic contact layer pattern 57 and the semiconductor pattern 42. The semiconductor pattern 42 may also be formed to have a uniform thickness by etching with the gas mixture of CF_4 and O_2. At this time, as shown in FIG. 12B, the thickness of the semiconductor pattern 42 may be reduced and the second portion 112 of the photoresist pattern is also etched to a certain thickness. The etch conditions may also be set not to etch the gate insulating layer 30, and it is preferable to make the photoresist pattern thick enough not to expose the data wire parts 62, 64, 65, 66, and 68.

As a result, the source electrode 65 and the drain electrode 66 are separated, and the data wire parts 62, 64, 65, 66, and 68 and the underlying contact layer patterns 55, 56, and 58 are completed.

Next, the remaining second portion 112 of the photoresist layer on the data

wire (Region A of FIG. 6C) is removed. However, the second portion 112 may be removed after removing the conductor pattern 67 for source/drain electrodes on the channel part C of FIG. 11B and before removing of the ohmic contact layer pattern 57 under the conductor pattern 67.

To summarize, this process can be done by using both wet etching and dry etching in turn, or by using only dry etching.

In the former case, the conductor layer of the part B is first removed by wet etching, and then the underlying ohmic contact layer and the semiconductor layer are removed by dry etching. At this time, the photoresist layer of the part C is consumed to a certain thickness, and the part C may have or may not have any residual photoresist left, which substantially depends on the initial thickness of the photoresist layer of the part C. When the part C has residual photoresist left, this residual photoresist is removed by ashing. Finally, the conductor layer of the part C is wet etched to separate the source and the drain electrodes, and the ohmic contact layer of the part C is removed by using dry etching.

In the latter case, the conductor layer, the ohmic contact layer, and the semiconductor layer of the part B are removed by dry etching. As in the former case, the part C may have or may not have residual photoresist left, and residual photoresist is removed by ashing when part C does have any residual photoresist. Finally, the conductor layer of the part C is dry etched to separate the source and the drain electrodes, and the ohmic contact layer of the part C is removed by dry etching.

Also, if the data wire is etched, the semiconductor pattern, the contact layer pattern, and the data wire may be completed in the same step at once. That is to

say, it is desirable that the photoresist pattern 114 and the underlying contact layer 50 of the part C are dry etched, and the portion of the photoresist pattern 112 of the part A is dry etched during the dry etching of the conductor layer, the ohmic contact layer, and the semiconductor layer of the part B.

Since the latter process uses only one type of etching method, it is simpler, although it is harder to achieve proper etching conditions. On the other hand, the former process can easily meet the proper etching condition, although more complicated.

After forming data wire parts 62, 64, 65, 66, and 68, photoresist layers including red, green, and blue resins are coated on the substrate and patterned to form color filters 75, 77, and 79 through photolithography processes using a third mask, a fourth mask and a fifth mask as shown in FIGs. 13A to 13C. At this time, contact holes 71, 72, 73, and 74 respectively exposing the drain electrode 66, the gate pad 24, the data pad 64, and the conductor pattern 68 for the storage capacitor are formed. Here, it is preferable that the color filters 75, 77, and 79 completely cover the data line 62. In this embodiment, the color filters 75, 77, and 79 do not overlap each other. However, it is preferable that the color filters 75, 77, and 79 overlap each other to prevent gate wire defects and data wire defects in the later manufacturing process. The overlap of the gate line 22 and the data line 62, and the intersections of the color filters 75, 77, and 79 and the gate line 22 and the data line 62 may form a very steep step. However, these deep steps may be moderated by using a mask having partially different transmittances when forming the color filters 75, 77, and 79. A planarization step may be added to flatten these steps.

Next, as shown in FIGs. 1 to 3, an ITO layer is deposited to a thickness of

400 Å to 500 Å, and etched by using a sixth mask to form a pixel electrode 82, a redundant gate pad 84, and a redundant data pad 86.

In this embodiment, by forming the data wire parts 62, 64, 65, 66, and 68, the ohmic contact layer pattern 55, 56, and 58, and the semiconductor patterns 42 and 48 through one photolithography process, and the red, green, and blue color filters 75, 77, and 79 as a passivation layer, an LCD panel having thin film transistor and color filters together may be completed in just six photolithography processes

In this embodiment, the red, green, and blue color filters 75, 77, and 79 are used as a passivation layer, but another passivation layer may be added. In this method, the passivation layer must be etched to form contact holes 71, 72, 73, and 74 respectively exposing the drain electrode 66, the gate pad 24, the data pad 64, and the conductor pattern 68 for the storage capacitor. In this case, the gate insulating layer 30 may not be etched when etching the conductor layer 60 and the underlying layers using the photoresist patterns 112 and 114 as an etch mask in the second photolithography step. Instead, the gate insulating layer 30 is etched along with the passivation layer to form contact holes 71, 72, 73, and 74. This method will be described below.

First, the structure of the thin film transistor panel for a liquid crystal display of the second embodiment according to the present invention will be described with reference to FIGs.14 and 16.

FIG. 14 is a layout view of a thin film transistor array panel for a liquid crystal display according to the second embodiment of the present invention, and FIGs. 15 and 16 are cross-sectional views taken along lines XV-XV' and XVI-XVI' of FIG. 14, respectively.

Most of the structure is similar to the first embodiment.

Gate wires 22, 24, and 26, and a storage electrode 28 are made of a conductive material having some degrees of photosensitivity.

A gate insulating layer 30 of silicon-nitride (SiNx) covering the gate wire parts 22, 24, and 26, and the storage electrode 28 is formed on the whole surface of an insulating substrate 10.

Also, data wires 62, 64, 65, and 66, and a conductor pattern 68 for a storage capacitor, which are formed on an ohmic contact layer patterns 55, 56, and 58, are made of a conductive material having some degrees of photosensitivity.

Here, the data wires 62, 64, 65, and 66, the conductor pattern 68, the gate wires 22, 24, and 26, and the storage electrode 28 are made of a photosensitive conductive material. However, like the first embodiment, they may be made of metal or conductive material such as aluminum (Al) or aluminum alloy, molybdenum (Mo) or molybdenum-tungsten (MoW), chromium (Cr), and tantalum (Ta) and may have a multiple-layered structure. Of course, in a multiple-layered structure, it is preferable that one layer is made of a material having a low resistivity and another layer is made of a material having good contacting properties.

Red, blue, and green color filters 75, 77, and 79 are made of photosensitive material and are formed on the data wire parts 62, 64, 65, 66, and 68, and the gate insulating layer 30 that is not covered by the data wire parts 62, 64, 65, 66, and 68. The color filters 75, 77, 79 that have contact holes 71, 72, 73, and 74 are covered by a passivation layer 90, which is made of organic insulating material and is planarized.

The red, blue, and green color filters 75, 77, and 79, and the passivation layer

90 have contact holes 91, 93, and 94 respectively exposing the drain electrode 66, the data pad 64 and the conductor pattern 68 for storage capacitor, and contact hole 92 exposing the gate pad 24.

Pixel electrodes 82, which receive an image signal and generate an electric field with a common electrode of an upper panel, are formed on the passivation layer 90. The pixel electrode 82 is made of a transparent conductive material such as indium tin oxide (ITO). The pixel electrode 82 is connected to the drain electrode 66 both physically and electrically through the contact hole 71, and receives image signals from the drain electrode. Even though the aperture ratio increases by overlapping the pixel electrode 82 on the gate lines 22 or the adjacent the data lines, these lines are not required to be overlapped by the pixel electrode. The pixel electrode 82 is connected to the conductor pattern 68 for the storage capacitance through the contact hole 74 and transmits the image signals to the conductor pattern 68.

A redundant gate pad 84 and a redundant data pad 86 respectively connected to the gate pad 24 and the data pad 64 through the contact holes 72 and 73 are formed on the gate pad 24 and the data pad 64. These redundant pads 84 and 86 are optional as they protect the pads 24 and 64 from corrosion by the ambient air and strengthens the adhesion between the external circuit and the pads 24 and 64.

A method for manufacturing a thin film transistor array panel according to a second embodiment of the present invention will now be described with reference to the FIGs. 17A to 20C and FIGs. 14 to 16.

At first, as shown in FIGs. 17A and 17B, a photosensitive conductive layer is laid on a substrate 10 to a thickness of 2,000 Å to 10,000 Å, and gate wire parts

including a gate line 22 having a gate electrode 26, a gate pad 24, and a storage electrode 28 are formed only by exposure and development through a photolithography process using a mask. When forming the gate wires here, the gate wires may be formed through a photolithography process using a photoresist pattern. However, if a photosensitive conductive layer is used, like in this second embodiment, an etch step using the photoresist pattern as an etch mask may be omitted, and the gate wires 22, 24, 26, and 28 may be formed by a photolithography process that includes only exposure and development steps. Accordingly, the manufacturing process can be simplified.

An example of a photosensitive conductive layer is an Ag paste photoresist mixture, and photosensitive Ag paste may be coated on the substrate 10 through screen printing.

The photosensitive conductive layer may be an organic metal layer formed through metal organic chemical vapor deposition. In copper organic metal, for example, copper atoms are intertwined with organic molecules. A photosensitive conductive layer may be formed by mixing photoresist materials with such a copper organic metal, and depositing the mixture onto the substrate.

Next, as shown in FIGs. 18A and 18C, a gate insulating layer 30, a semiconductor layer 40, and an ohmic contact layer 50 are sequentially deposited to thicknesses of 1,500 Å to 5,000 Å, 500 Å to 2,000 Å, and 300 Å to 600 Å, respectively, by such methods as chemical vapor deposition (CVD). Then, a data conductor layer, such as a photosensitive conductive material is formed to a thickness of 10,000 Å to 20,000 Å, and is exposed to light through a second mask and developed to form a data wire pattern 67 and 68. At this time, the first portion of

the data wire pattern located between a source electrode 65 and a drain electrode 66, i.e., a thin film transistor channel part C as shown in FIG. 18C, is thinner than the second portion of the data wire pattern located over the data wire portion A where a data wire parts 62, 64, 65, 66, and 68 will be formed. The third portion, the remaining portion located at portion B, is where a data conductor layer is completely removed, as with the photoresist patterns 112 and 114 of the first embodiment. The method forming the data wire patterns 67 and 68 having different thicknesses depending on positions is the same as that of the first embodiment.

Next, as shown in FIGs. 19A and 19B, the data wire patterns 67 and 68, and the underlying layers including the ohmic contact layer 50 and the semiconductor layer 40 are then subject to an etching process. Finishing this step, the data wire pattern and the underlying layers at the data wire part A, as well as only the semiconductor layer on the channel part C remain. In addition, the layers 50 and 40 in the remaining part B are removed from the gate insulating layer 30.

As shown in FIGs. 19A and 19B, the gate insulating layer 30 is exposed by removing the ohmic contact layer 50 and the semiconductor layer 40 of the part B, and semiconductor patterns 42 and 48 are completed. At this time, the data wire pattern 67 of the channel portion C is etched and is removed. Next, the data wire pattern 67 of the channel portion C is completely removed by dry-etch. The underlying ohmic contact layer 50 is removed to complete the data wire including the data line 62, the data pad 64, the source electrode 65, the drain electrode 66, and the conductor pattern 68 for storage capacitor, and the underlying ohmic contact layer patterns 55, 56, and 58. At this time, the data wire 62, 64, 65, and 66, and the conductor pattern for a storage capacitor is also etched to a certain thickness. Here,

it is preferable that the etch condition is controlled not to etch the gate insulating layer 30.

After forming data wire parts 62, 64, 65, 66, and 68, the ohmic contact layer patterns 55, 56, and 58, and the semiconductor patterns 42 and 48 by the above steps, photosensitive photoresist layers including red, green, and blue resins are coated by screen printing or off-set printing, and patterned to form color filters 75, 77, and 79, as shown in FIGs. 20A to 20C.

Next, a passivation layer 90 covering the color filters 75, 77, and 79 is formed on the substrate 10, and exposed and developed along the color filters 75, 77, and 79 through photolithography step using a mask to form contact holes 91, 92, 93, and 94 respectively exposing the drain electrode 66, the gate insulating layer 30 on the gate pad 24, the data pad 64, and the conductor pattern 68 for the storage capacitor. Then, the gate insulating layer 30 that is not covered by the passivation layer 90 is etched to expose the gate pad 24 through the contact hole 92. At this time, it is preferable that the passivation layer 90 is made of organic transparent material having good planarization and photosensitive properties. It may lower the step that forms by the layer to be laid later. The contact holes 91, 92, 93, and 94 may be formed through a photolithography process using only exposure and development by patterning along with the color filters 75, 77, and 79. If the contact holes 91, 92, 93, and 94 may be formed in the step of printing the color filters 75, 77, and 79, the passivation layer 90 may be omitted. As with this embodiment, when forming the passivation layer 90, it is easy to control the thickness of the passivation layer 90 and the color filters 75, 77, and 79, and to form the contact holes 91, 92, 93, and 94 through a photolithography process using only exposure and development.

However, the downside of printing method forming the color filters 75, 77, and 79 is a low resolution. The reference number 100 in FIG. 20A indicates the boundary of the color filters 75, 77, and 79. Furthermore, the color filters 75, 77, and 79 may overlap each other.

Next, as shown in FIGs. 14 to 16, an ITO layer is deposited to a thickness of 400 Å to 500 Å, and etched by using a mask to form a pixel electrode 82, a redundant gate pad 84, and a redundant data pad 86.

On the other hand, a light blocking layer to absorb or block light such as ultraviolet rays or visible rays of short-wave lengths, which may reach the channel portion of the thin film transistor from outside, can be formed of color filters without additional steps. It will be described referring to drawings.

FIG. 21 is a layout view of a thin film transistor array panel for a liquid crystal display according to the third embodiment of the present invention, and FIGs. 22 and 23 are cross-sectional views taken along lines XXII-XXII' and XXIII-XXIII' of FIG. 21, respectively.

As shown in FIGs. 21 to 23, most of the structure is the same as the second embodiment.

However, a light blocking layer 78 to absorb or block lights such as ultraviolet rays or visible rays of short-wave lengths, which may reach the channel portion C of the thin film transistor from outside, is formed with the same layer as the color filters 75, 77, and 79 over the channel portion C of the thin film transistor. The light blocking layer 78 may be located on or under the color filters 75, 77, and 79 depending on the order how the color filters 75, 77, and 79 are formed. In order to absorb as much lights as possible combing from outside, it is desirable that the light

blocking layer has a single-layered or double-layered structure of the red color filter and/or the green color filter, so that the light goes through the red and green color filters. The light blocking layer 78 over the channel portion C, by absorbing or blocking the lights such as ultraviolet rays or visible rays of short-wave lengths, minimizes the leakage current at channel portion of the thin film transistor and improves the display quality.

Most of the manufacturing method according to the third embodiment is similar to the second embodiment.

However, when forming the red, green, blue color filters 75, 77, and 79, the light blocking layer 78 made of the red or green color filters is formed over the channel portion C of the thin film transistor. Here, the light blocking layer 78 may be located on or under the color filters 75, 77, and 79 depending on the order how the color filters 75, 77, and 79 are formed. Also, in order to absorb as much lights as possible, it is desirable that the light, which are incident to the channel portion C of the thin film transistor, goes through the red and green color filters.

Next, like the second embodiment, a passivation layer 90, acrylic organic material covers the color filters 75, 77, and 79, and the light blocking layer 78 is formed on the substrate 10. The passivation layer 90 is patterned along with the color filters 75, 77, and 79, and the gate insulating layer 30 through photolithography step using a mask to form contact holes 91, 92, 93, and 94 respectively exposing the drain electrode 66, the gate pad 24, the data pad 64, and the conductor pattern 68 for the storage capacitor. It is preferable that the passivation layer 90 is made of material that can be easily planarized to flatten the steps of under-layers and then to minimize alignment distortions of liquid crystal molecules. The reference number

100 in FIG. 21 indicates the boundary of the color filters 75, 77, and 79. Furthermore, the color filters 75, 77, and 79 may overlap each other.

In this embodiment, a buffer insulating layer of such material as silicon nitride may be laid before forming the red, green, blue color filters 75, 77, 79, because it may prevent the channel portion C of the thin film transistor from contaminated by the photosensitive material including resins of the color filters.

Such a thin film transistor panel may be fabricated by many other different ways and involve many other alternative structures.

In this embodiment, the data wire parts, the ohmic contact layer patterns and the semiconductor patterns are formed through a photolithography process using one mask. Also, the gate wire and the data wire, made of photosensitive conductive material, are formed through a photolithography process without an etch step, simplifying the manufacturing process. Also, the methods according to the present invention reduces the number of masks employed in manufacturing a thin film transistor panel for a liquid crystal display and also minimizes the manufacturing costs. Also, the light blocking layer over the channel portion, by blocking or absorbing the lights such as ultraviolet rays or visible rays of short-wave lengths, which are incident to the channel portion C, minimizes the leakage current in channel portion of the thin film transistor and improves the display quality.

In the drawings and specification, there have been disclosed typical preferred embodiments of the present invention and, although specific terms are employed, they are used in a generic and descriptive sense only and not for purposes of limitation, the scope of the invention being set forth in the following claims.

WHAT IS CLAIMED IS:

1. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer pattern covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming an ohmic contact layer pattern on the semiconductor pattern;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on the ohmic contact layer;

forming red, green, and blue color filters, said color filters covering the data wire and having a first contact hole exposing the drain electrode; and

forming a pixel electrode connected to the drain electrode through the first contact hole,

wherein the source electrode and the drain electrode are separated by a photolithography process using a photoresist pattern, and the photoresist pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness larger than the first portion, and a third portion having a third thickness smaller than the first thickness.

2. The method of claim 1, wherein the photoresist pattern is formed by a mask that has a first, a second, and a third part, a transmittance of the third part is higher than the first and the second parts, a transmittance of the first part is higher than the second part, and

wherein the photoresist pattern is made of positive photoresist, and the mask is aligned such that the first, the second, and the third parts respectively face the first, the second, and the third portions of the photoresist pattern in an exposing step.

3. The method of claim 2, wherein the first part of the mask includes a partially transparent layer.

4. The method of claim 2, wherein the first part of the mask includes a pattern smaller than the resolution of the exposure used in the exposing step.

5. The method of claim 1, wherein the first portion is formed by reflow.

6. The method of claim 1, wherein the thickness of the first portion is less than a half of the thickness of the second portion.

7. The method of claim 6, wherein the thickness of the second portion is 1μ to 2μ.

8. The method of claim 7, wherein the thickness of the first portion is less than 4,000 Å.

9. The method of claim 1, wherein the data wire, the ohmic contact layer pattern, the semiconductor pattern, and the gate insulating layer pattern are formed in the same photolithography process.

10. The method of claim 9, wherein steps of forming the gate insulating layer pattern, the semiconductor pattern, the ohmic contact layer pattern, and the data wire comprises:

depositing a gate insulating layer, a semiconductor layer, an ohmic contact layer, and a conductor layer;

coating a photoresist layer on the conductor layer;

exposing the photoresist layer through a mask;

forming the photoresist pattern such that the second portion lies on the data wire by developing the photoresist layer;

forming the data wire, the ohmic contact layer pattern, the semiconductor pattern, and the gate insulating layer pattern that are respectively made of the conductor layer, the ohmic contact layer, the semiconductor layer, and the gate insulating layer by removing a portion of the conductor layer under the third portion, the semiconductor layer, the ohmic contact layer, and the underlying gate insulating layer, and by removing the first portion, the conductor layer, and the ohmic contact layer under the first portion, and by removing a partial thickness of the second portion; and

removing the photoresist pattern.

11. The method of claim 10, wherein the step of forming the data wire, the ohmic contact layer pattern, the semiconductor pattern, and the gate insulating layer pattern comprises:

removing the portion of the conductor layer under the third portion by dry etching or wet etching to expose the ohmic contact layer;

dry etching the ohmic contact layer under the third portion, the semiconductor layer, and the underlying gate insulating layer, and the first portion to complete a semiconductor pattern and a gate insulating layer pattern, along with exposing the substrate or the gate insulating layer under the third portion and the conductor layer under the first portion; and

removing the conductor layer under the first portion and the underlying ohmic contact layer to complete a data wire and a ohmic contact layer pattern.

12. The method of claim 1, wherein the gate wire further includes a gate pad

that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and the color filters have a second contact hole and a third contact hole respectively exposing the gate pad and the data pad,

further comprising a step of forming a redundant gate pad and a redundant data pad that are made of the same layer as the pixel electrode and are respectively connected to the gate pad and the data pad through the second contact hole and the third contact hole.

13. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on the ohmic contact layer;

forming a passivation layer covering the data wire and having a first contact hole exposing the drain electrode; and

forming a pixel electrode connected to the drain electrode through the first contact hole,

wherein the data wire or the gate wire is made of a photosensitive conductive material.

14. The method of claim 13, wherein the source electrode and the drain electrode are separated by a photolithography process using a data wire pattern,

and the data wire pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

15. The method of claim 14, wherein the data wire pattern is formed by a mask that has a first, a second, and a third part, a transmittance of the third part is higher than the first and the second parts, a transmittance of the first part is higher than the second part, when the data wire pattern contains a positive photoresist material, and the mask is aligned such that the first, the second, and the third parts respectively face the first, the second, and the third portions of the data wire pattern in an exposing step.

16. The method of claim 15, wherein the first part of the mask includes a partially transparent layer.

17. The method of claim 15, wherein the first part of the mask includes a pattern smaller than the resolution of the exposure used in the exposing step.

18. The method of claim 13, further comprising the step of forming an ohmic contact layer pattern between the data wire and the semiconductor.

19. The method of claim 18, wherein the data wire, the ohmic contact layer pattern, and the semiconductor pattern are formed in the same photolithography process.

20. The method of claim 19, wherein steps of forming the semiconductor pattern, the ohmic contact layer pattern, and the data wire comprise:

depositing a semiconductor layer, an ohmic contact layer, and a data conductor layer on the gate insulating layer:

exposing the data conductor layer through a mask;

forming the data wire pattern such that the second portion lies on the data wire by developing the data conductor layer;

forming the data wire, the ohmic contact layer pattern, and the semiconductor pattern respectively made of the data conductor layer, the ohmic contact layer, and the semiconductor layer by removing a portion of the ohmic contact layer under the third portion and the underlying semiconductor layer, the first portion and the ohmic contact layer under the first portion, and a partial thickness of the second portion.

21. The method of claim 20, wherein the step of forming the data wire, the ohmic contact layer pattern, and the semiconductor pattern comprises;

removing the portion of the ohmic contact layer under the third portion and the semiconductor layer by dry etching along the first portion to expose the gate insulating layer and to complete the semiconductor pattern made of the semiconductor layer, and

removing the data conductor layer under the first portion and the underlying ohmic contact layer to complete a data wire and an ohmic contact layer pattern.

22. The method of claim 21, further comprising the step of forming red, green, and blue color filters before forming the passivation layer.

23. The method of claim 22, wherein the red, green and blue color filters are coated by screen printing or off-set printing.

24. The method of claim 23, wherein the red, green, and blue color filters, and the passivation layer are made of a photosensitive material.

25. The method of claim 24, wherein the red, green, and blue color filters, and the passivation layer are patterned through only exposure and development.

26. The method of claim 13, wherein the gate wire and the data wire are patterned through only exposure and development.

27. The method of claim 13, wherein the gate wire further includes a gate pad that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and the passivation layer and the gate insulating layer have a second contact hole and a third contact hole respectively exposing the gate pad and the data pad,

further comprising a step of forming a redundant gate pad and a redundant data pad that are made of the same layer as the pixel electrode and respectively connected to the gate pad and the data pad through the second contact hole and the third contact hole.

28. The method of claim 13, wherein the photosensitive conductive material is made of Ag paste or copper organic metal that include photoresist.

29. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a data line connected to the source electrode on the ohmic contact layer;

forming red, green, and blue color filters, said filters made of photosensitive material and covering the data wire and having a first contact hole; and

forming a pixel electrode connected to the drain electrode through the first contact hole of the color filters.

30. The method of claim 29, wherein the red, green and blue color filters are coated through screen printing or off-set printing.

31. The method of claim 29, further comprising a step of forming a passivation layer covering a color filter before forming red, green, and blue color filters.

32. The method of claim 31, wherein the passivation layer is made of photosensitive transparent organic material having a good planarization property.

33. The method of claim 32, wherein the red, green, and blue color filters, and the passivation layer are patterned through only exposure and development to form the first contact hole.

34. The method of claim 33, wherein the gate wire further includes a gate pad that is connected to and receives a signal from an external circuit, and the data wire further includes a data pad that is connected to and receives a signal from an external circuit, and the color filter, the passivation layer, and the gate insulating layer have a second contact hole and a third contact hole respectively exposing the gate pad and the data pad,

further comprising a step of forming a redundant gate pad and a redundant data pad that are made of the same layer as the pixel electrode and respectively connected to the gate pad and the data pad through the second contact hole and the third contact hole.

35. The method of claim 29, wherein the gate wire or the data wire is made of photosensitive conductive material.

36. The method of claim 35, wherein the gate wire and the data wire are patterned through only exposure and development.

37. The method of claim 36, wherein the gate wire and the data wire are made of Ag paste or copper organic metal that includes photoresist.

38. The method of claim 29, wherein the source electrode and the drain electrode are separated by a photolithography process using a data wire pattern, and the data wire pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

39. The method of claim 38, wherein a mask used for forming the data wire pattern has a first, a second, and a third part, a transmittance of the third part is higher than the first part and the second part, a transmittance of the first part is higher than the second part, the data wire pattern includes positive photoresist material and the mask is aligned such that the first, the second, and the third parts respectively face the first, the second, and the third portions of the data wire pattern in an exposing step.

40. The method of claim 39, wherein the first part of the mask includes a partially transparent layer.

41. The method of claim 39, wherein the first part of the mask includes a pattern smaller than the resolution of the exposure used in the exposing step.

42. The method of claim 39, further comprising a step of forming an ohmic contact layer pattern between the data wire and the semiconductor.

43. The method of claim 42, wherein the data wire, the ohmic contact layer

pattern, and the semiconductor pattern are formed in the same photolithography process.

44. The method of claim 43, wherein steps of forming the semiconductor pattern, the ohmic contact layer pattern, and the data wire comprise:

depositing a semiconductor layer, an ohmic contact layer, and a data conductor layer on the gate insulating layer:

exposing the data conductor layer through a mask;

forming the data wire pattern such that the second portion lies on the data wire by developing of the data conductor layer;

forming the data wire, the ohmic contact layer pattern, and the semiconductor pattern respectively made of the data conductor layer, the ohmic contact layer, and the semiconductor layer by removing a portion of the ohmic contact layer under the third portion and the underlying semiconductor layer, the first portion and the ohmic contact layer under the first portion, and a partial thickness of the second portion.

45. The method of claim 44, wherein the step of forming the data wire, the ohmic contact layer pattern, and the semiconductor pattern comprises;

removing the portion of the ohmic contact layer under the third portion and the semiconductor layer by dry etching along the first portion to expose the gate insulating layer and to complete the semiconductor pattern made of the semiconductor layer, and

removing the data conductor layer under the first portion and the underlying ohmic contact layer to complete the data wire and the ohmic contact layer pattern.

46. A thin film transistor array panel for a liquid crystal display, comprising:

a gate wire including a gate line and a gate electrode connected to the gate

line, and formed on an insulating substrate;

a gate insulating layer covering the gate electrode;

a semiconductor pattern formed on the gate insulating layer;

a data wire including a source electrode and a drain electrode, and a data line connected to the source electrode;

a passivation layer covering the data wire and having a first contact hole exposing the drain electrode; and

a pixel electrode connected to the drain electrode through the first contact hole,

wherein the gate wire or the data wire are made of photosensitive conductive material.

47. The thin film transistor array panel of claim 46, further comprising red, green, and blue color filters formed under the passivation layer.

48. The thin film transistor array panel of claim 47, wherein the passivation layer and the color filters are made of photosensitive material.

49. The thin film transistor array panel of claim 46, wherein the conductive material is made of Ag paste or copper organic metal that includes photoresist.

50. A method for manufacturing a thin film transistor array panel for a liquid crystal display, comprising steps of:

forming a gate wire including a gate line and a gate electrode connected to the gate line on an insulating substrate;

forming a gate insulating layer covering the gate wire;

forming a semiconductor pattern on the gate insulating layer;

forming a data wire including a source electrode and a drain electrode and a

data line connected to the source electrode;

forming red, green, and blue color filters, said color filters covering the data wire and made of photosensitive material including red, green, and blue resins;

forming a light blocking layer made of the photosensitive material and covering the semiconductor pattern between the source electrode and the drain electrode when forming red, green, and blue color filters;

forming a contact hole exposing the drain electrode in the color filters; and

forming a pixel electrode connected to the drain electrode through the contact hole.

51. The method of claim 50, wherein the red, green and blue color filters are coated through screen printing or off-set printing, or formed through exposure and development process.

52. The method of claim 50, further comprising a step of forming a passivation layer covering the color filters after forming the red, green, and blue color filters.

53. The method of claim 52, wherein the passivation layer is made of transparent organic material having good planarization properties.

54. The method of claim 50, further comprising a step of forming a buffer insulating layer before forming the red, green, and blue color filters.

55. The method of claim 50, wherein the light blocking layer is made of photosensitive material of red or green resins.

56. The method of claim 50, wherein the gate wire or the data wire are made of photosensitive conductive material.

57. The method of claim 56, wherein the gate wire and the data wire are

patterned through only exposure and development.

58. The method of claim 50, wherein the source electrode and the drain electrode are separated by a photolithography process using a data wire pattern, and the data wire pattern has a first portion having a first thickness and is at least located between the source electrode and the drain electrode, a second portion having a second thickness thicker than the first portion, and a third portion having a third thickness thinner than the first thickness.

59. A thin film transistor array panel for a liquid crystal display, comprising:

a gate wire including a gate line and a gate electrode connected to the gate line, and formed on an insulating substrate;

a gate insulating layer covering the gate wire;

a semiconductor pattern formed on the gate insulating layer;

a data wire including a source electrode and a drain electrode, and a data line connected to the source electrode and defining a pixel along with the gate line;

red, green and blue color filters made of photosensitive material including red, green and blue resins and respectively formed in the pixel;

a light blocking layer formed on the channel portion of the semiconductor pattern between the source electrode and the drain electrode and made of the photosensitive material; and

a pixel electrode connected to the drain electrode through a contact hole of the red, green and blue color filter.

60. The thin film transistor array panel of claim 59, further comprising a passivation layer that covers the red, green, and blue color filters, and the light blocking layer, and is planarized.

61. The thin film transistor array panel of claim 60, wherein the passivation layer is made of acrylic organic material.

62. The thin film transistor array panel of claim 59, wherein the data wire has the same shape as the semiconductor pattern except for a channel portion.

63. The method of claim 59, wherein the light blocking layer is made of photosensitive material of red or green resins.

ABSTRACT OF THE DISCLOSURE

Disclosed is a simplified method for manufacturing a liquid crystal display. A gate wire including a gate line, a gate pad, and a gate electrode are formed on a substrate. A gate insulating layer, a semiconductor layer, and an ohmic contact layer are sequentially deposited, and a photoresist layer is coated thereon. The photoresist layer is exposed to light through a mask and developed to form a photoresist pattern. At this time, a first portion of the photoresist pattern which is located between the source electrode and the drain electrode is thinner than a second portion which is located on the data wire, and the photoresist layer is totally removed on other parts. The thin portion is made by controlling the amount of irradiating light or by a reflow process to form a thin portion, and the amount of light is controlled by using a mask that has a slit, a small pattern smaller than the resolution of the exposure device, or a partially transparent layer. Next, the exposed portions of conductor layer are removed by wet etch or dry etch, and thereby the underlying ohmic contact layer is exposed. Then the exposed ohmic contact layer and the underlying semiconductor layer are removed by dry etching along with the first portion of the photoresist layer. The residue of the photoresist layer is removed by ashing. Source/drain electrodes are separated by removing the portion of the conductor layer at the channel and the underlying ohmic contact layer pattern. Then, the second portion of the photoresist layer is removed, and red, green, and blue color filters, a pixel electrode, a redundant gate pad, and a redundant data pad are formed.

FIG. 1

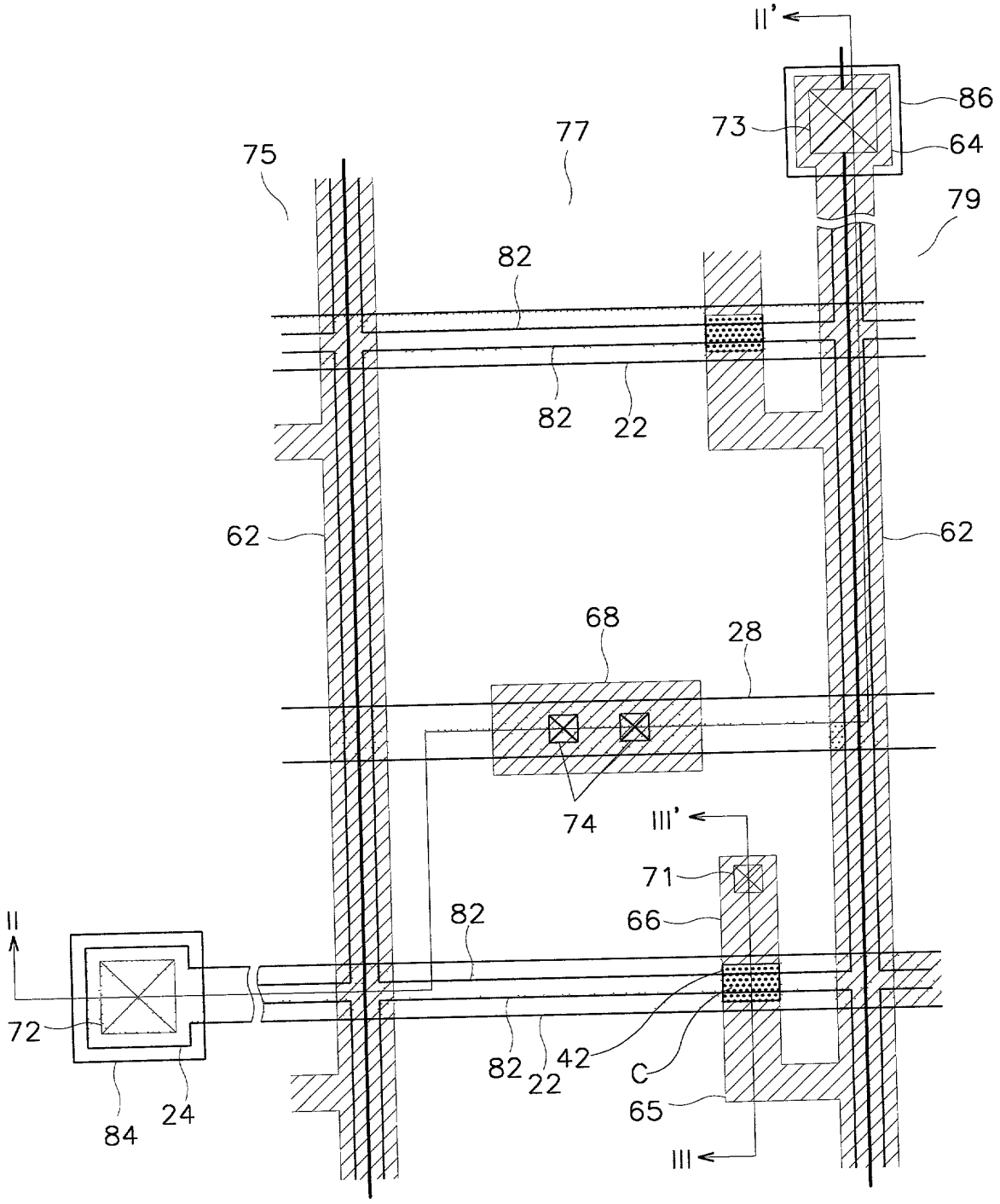
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FIG.2

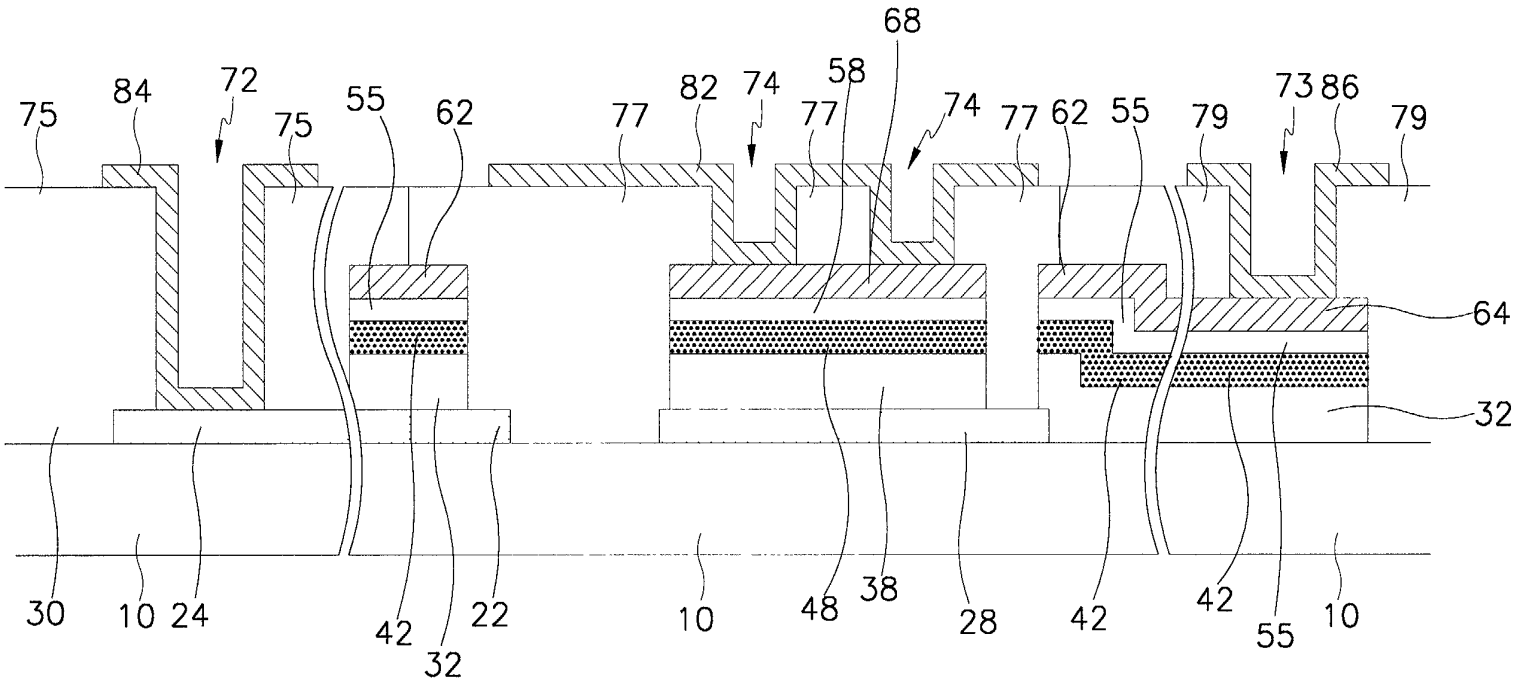
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FIG.3

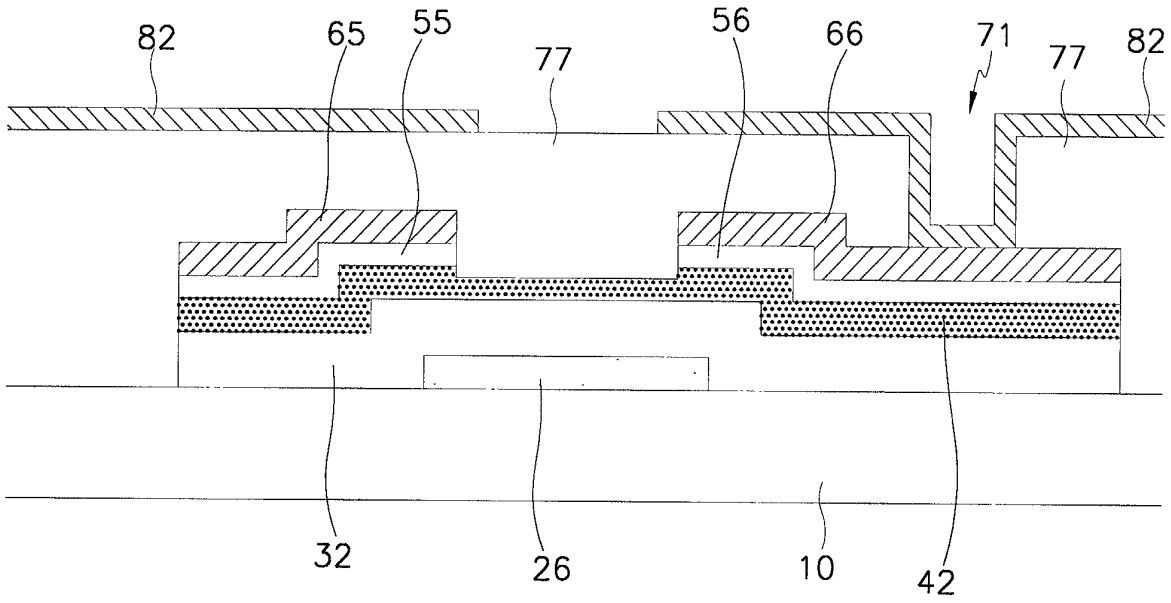

FIG.4A

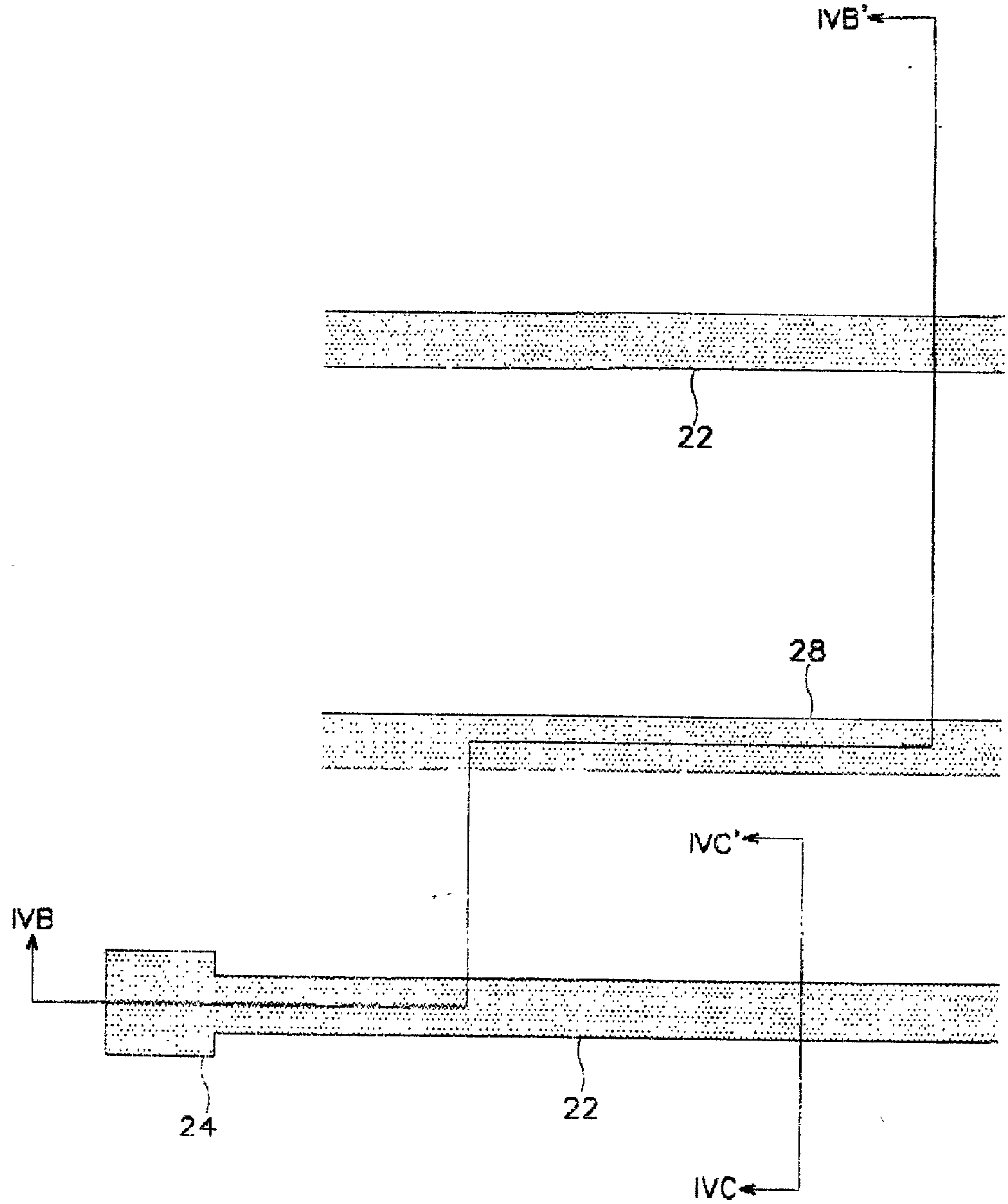

FIG.4B

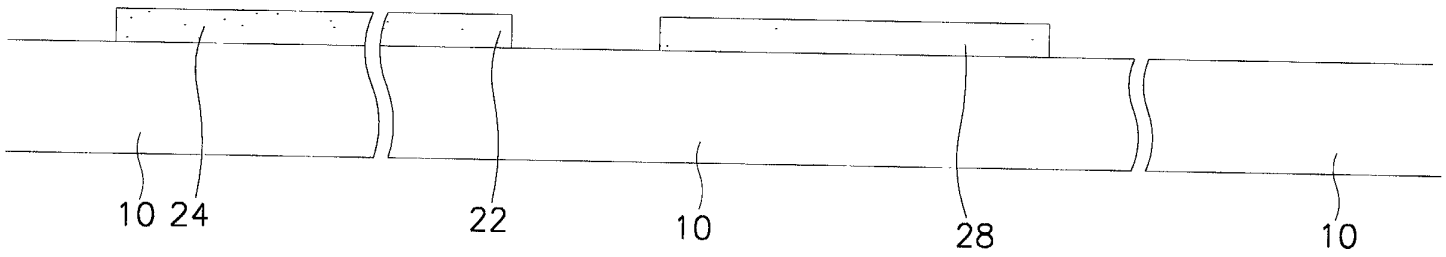

FIG.4C

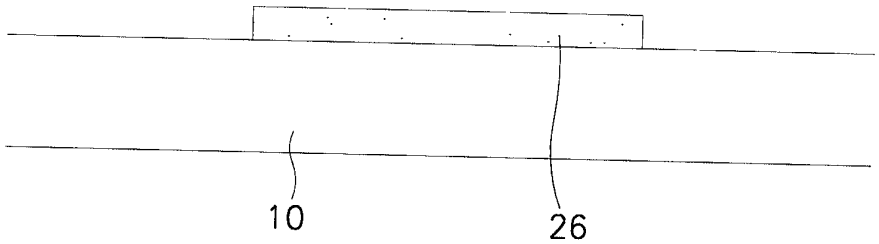

FIG.5A

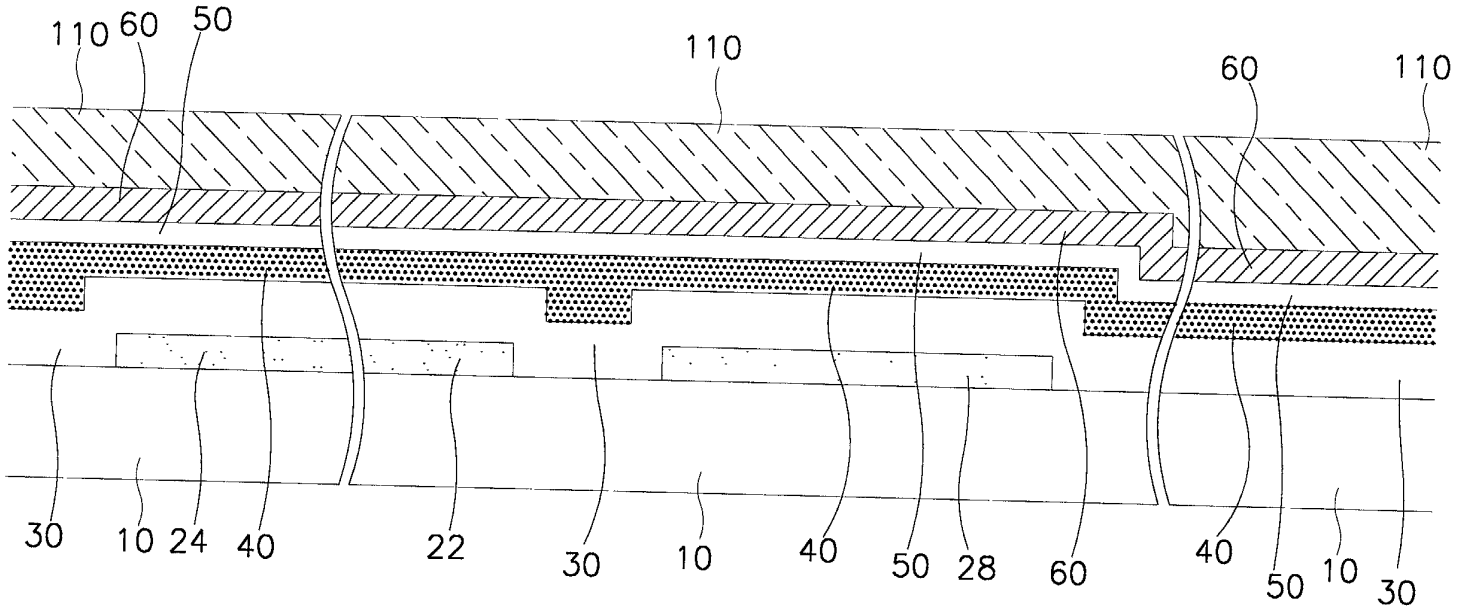

FIG.5B

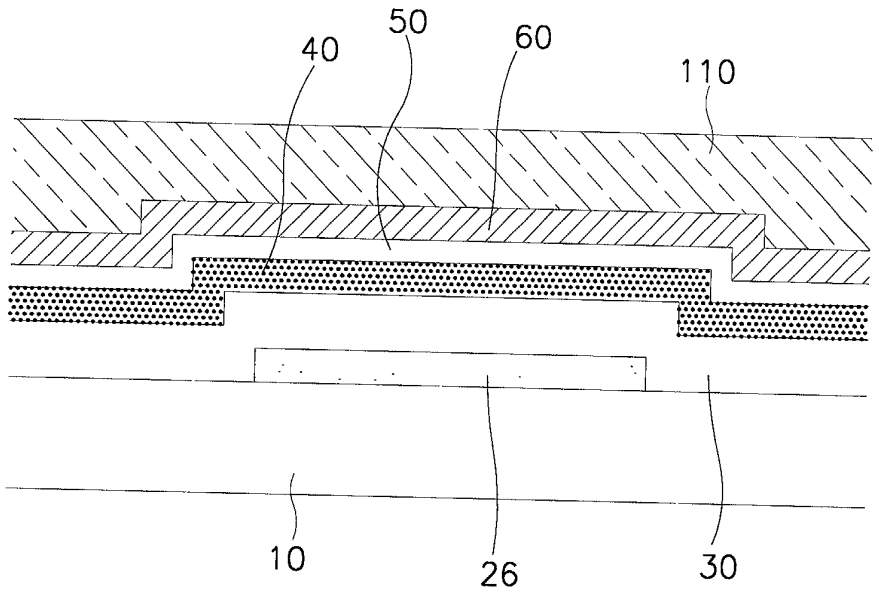

FIG.6A

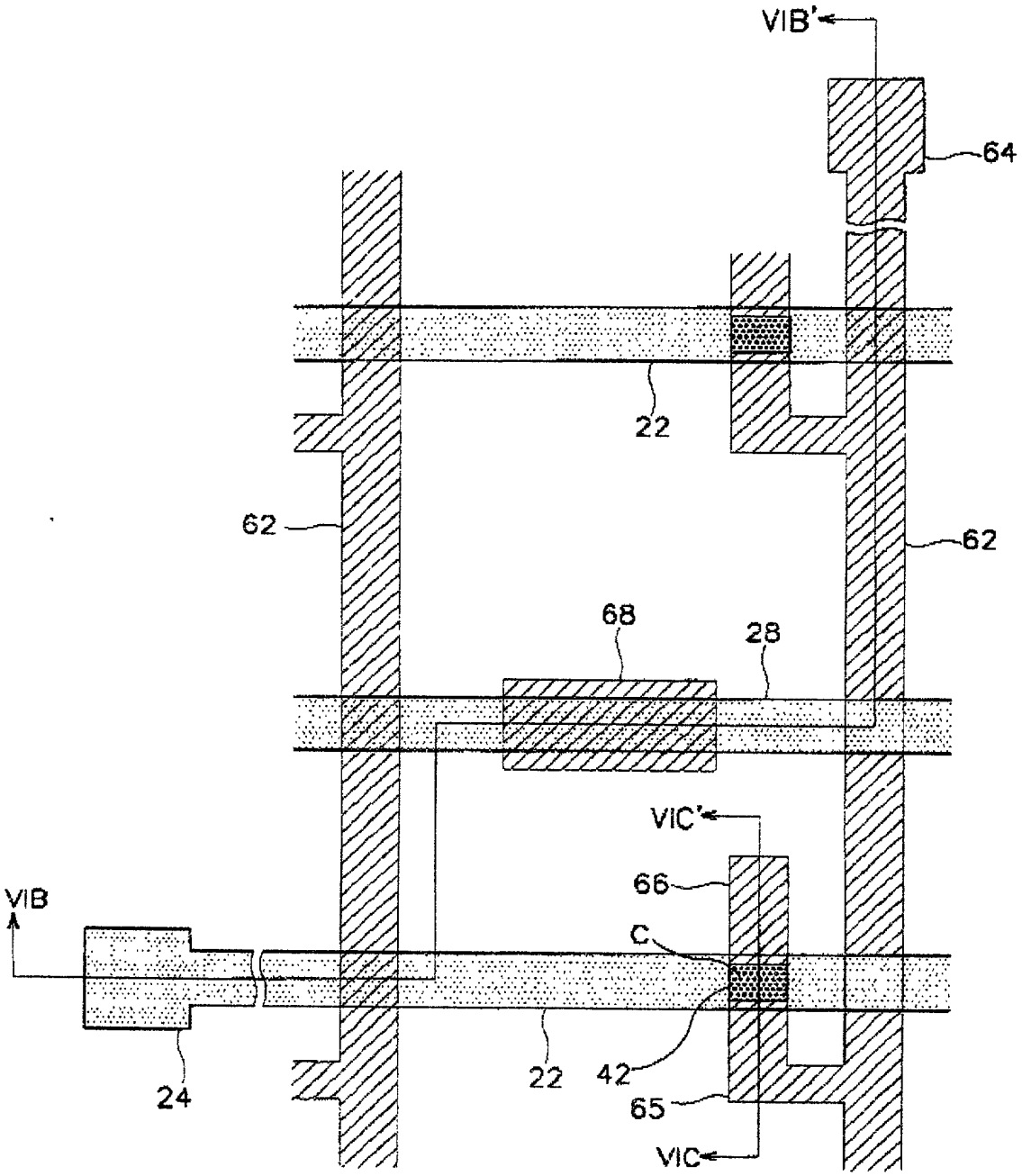

FIG.6B

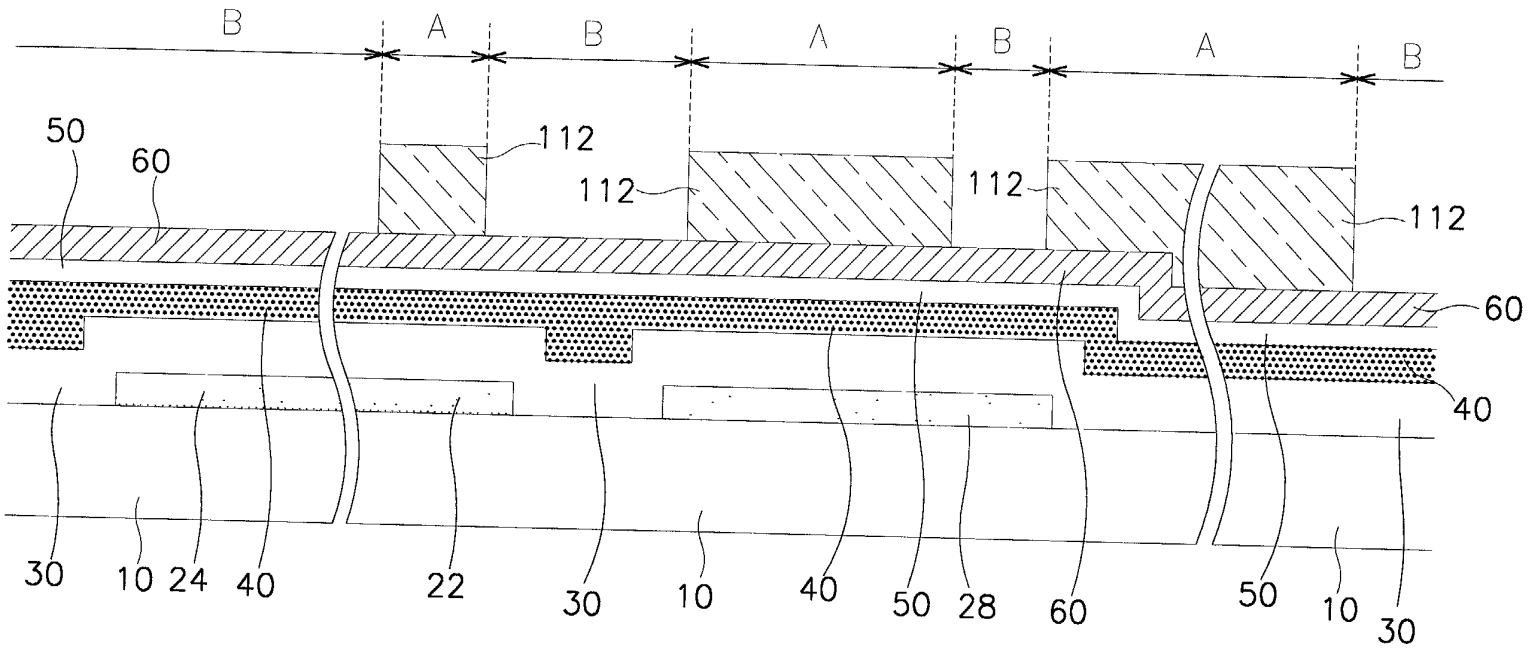
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FIG.6C

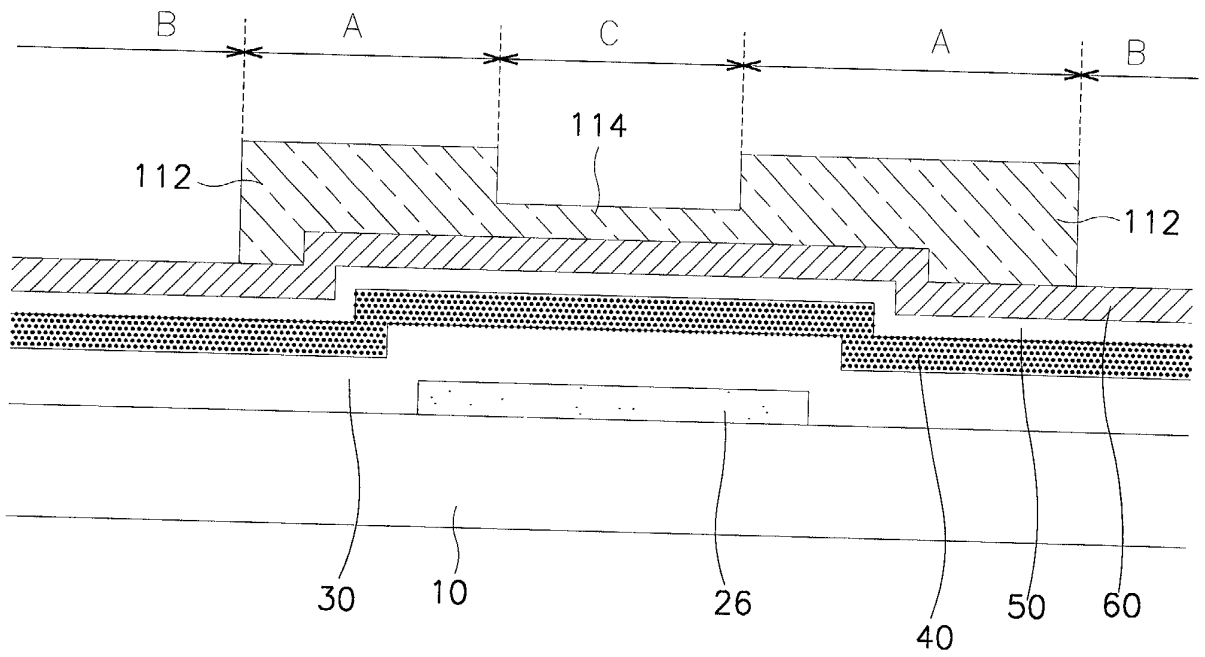


FIG.7A

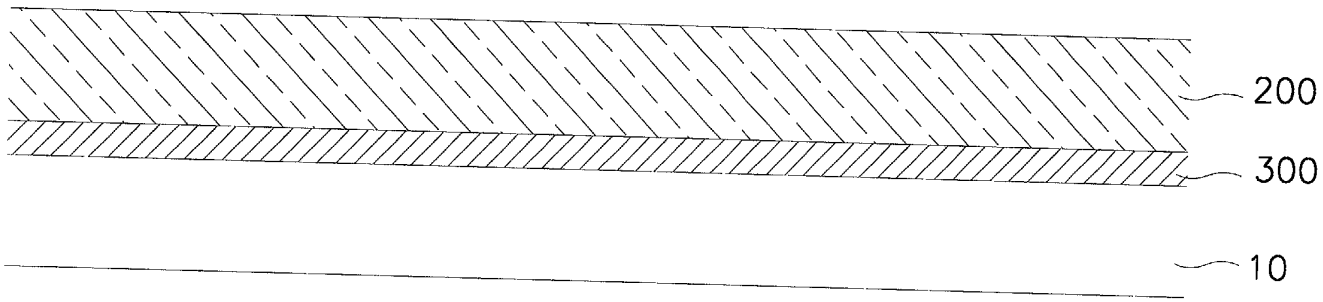


FIG.7B

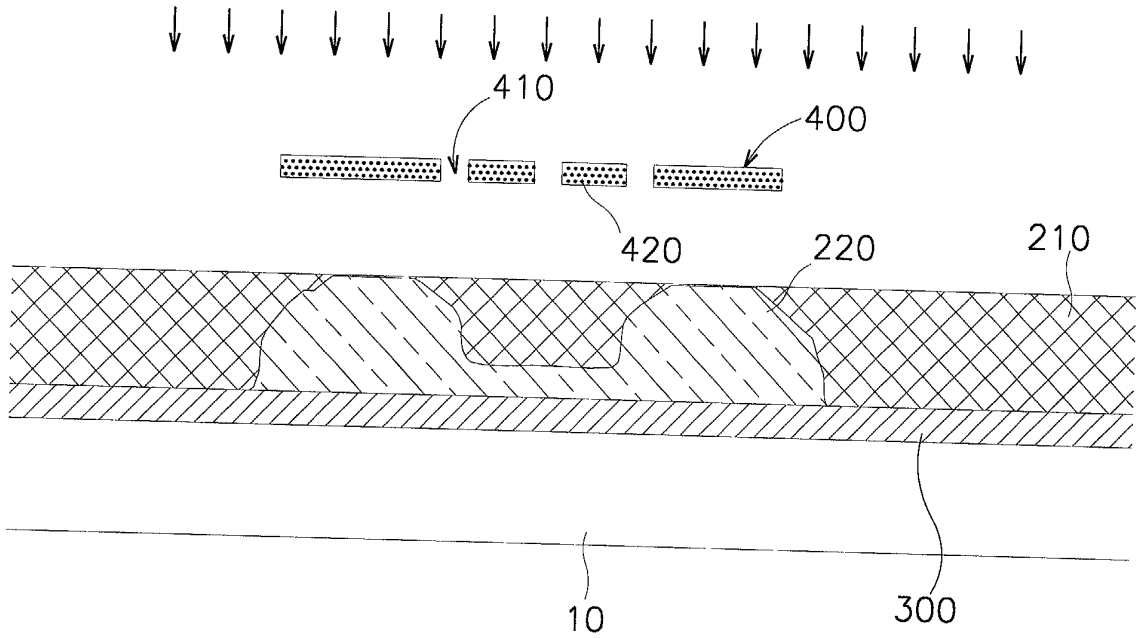


FIG.7C

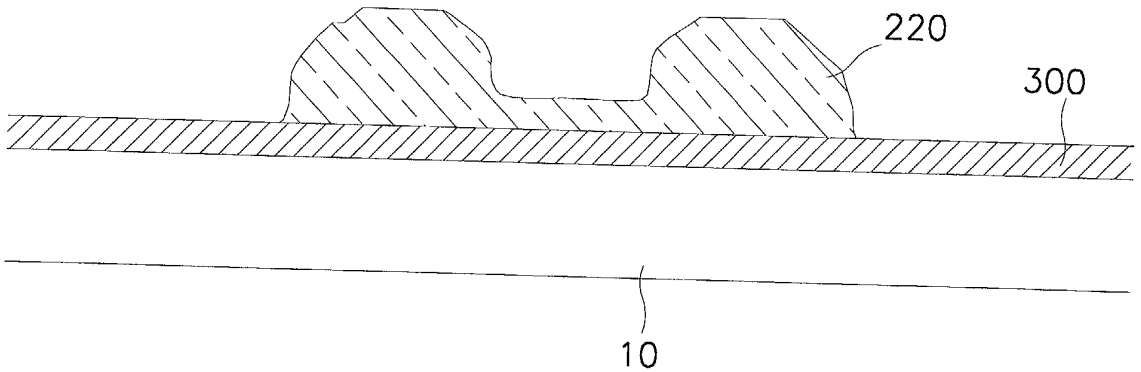
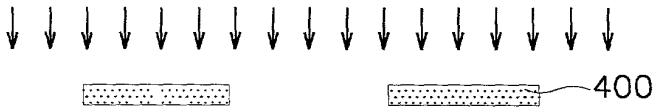


FIG.8A



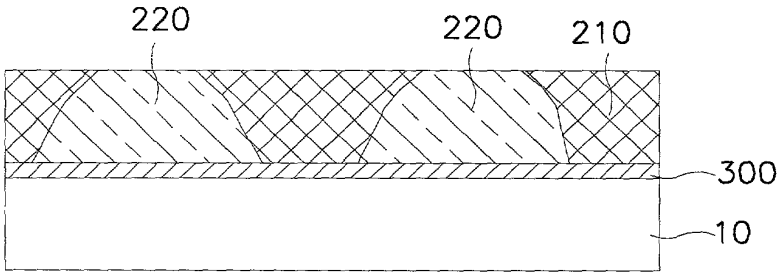


FIG.8B

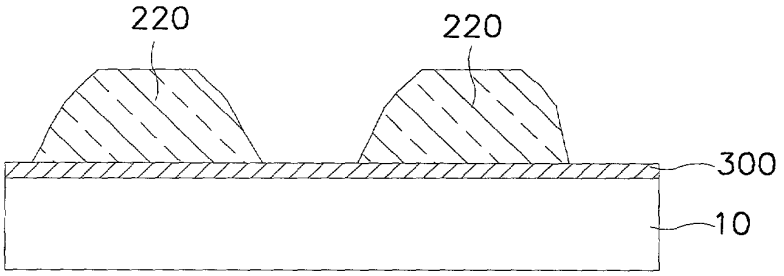


FIG.8C

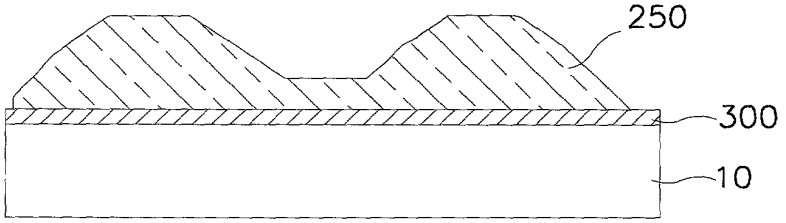


FIG.9A

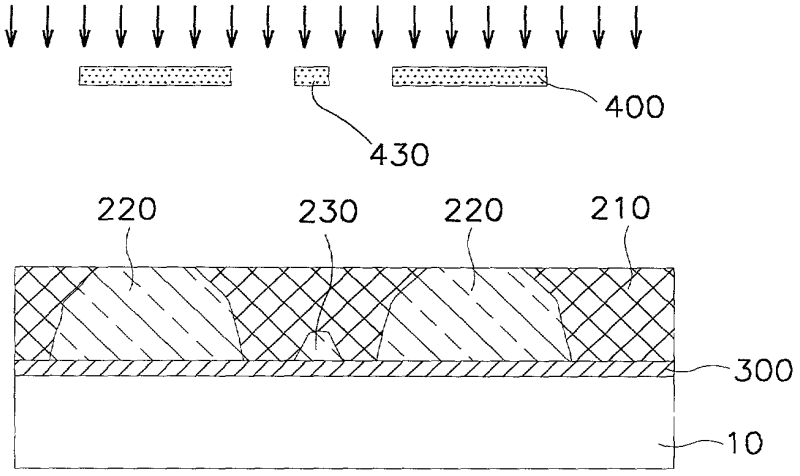


FIG.9B

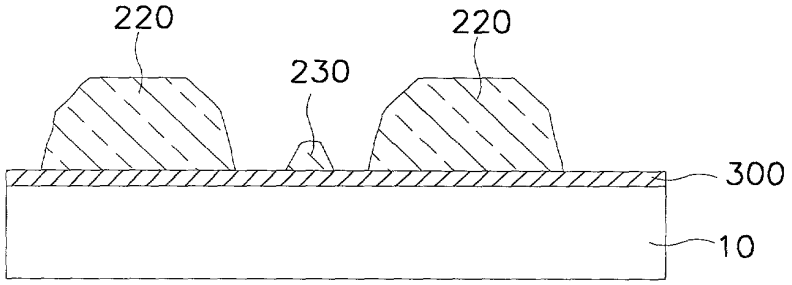


FIG.9C

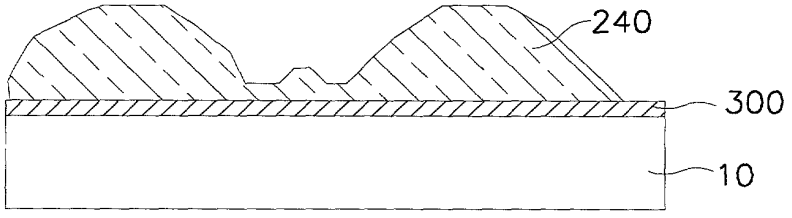


FIG.10A

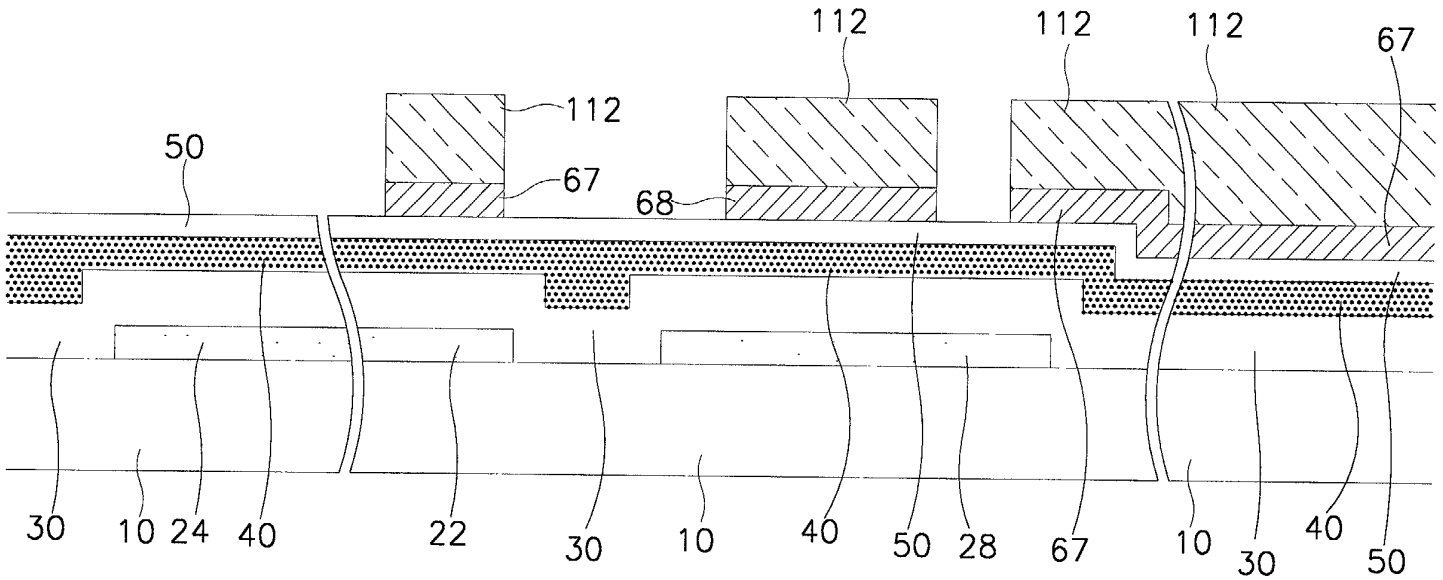

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FIG.10B

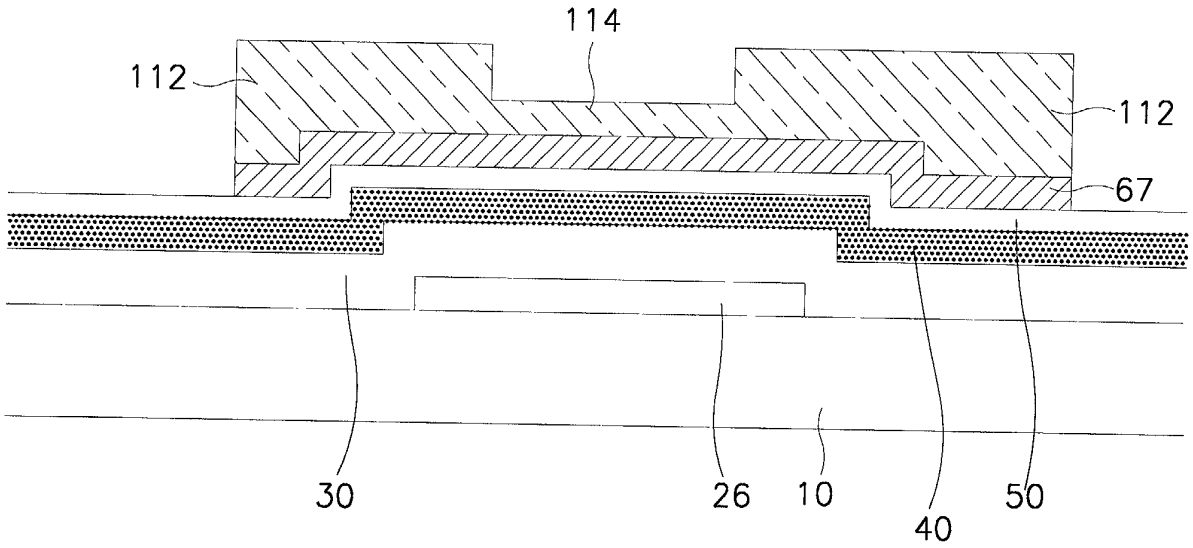

FIG. 11A

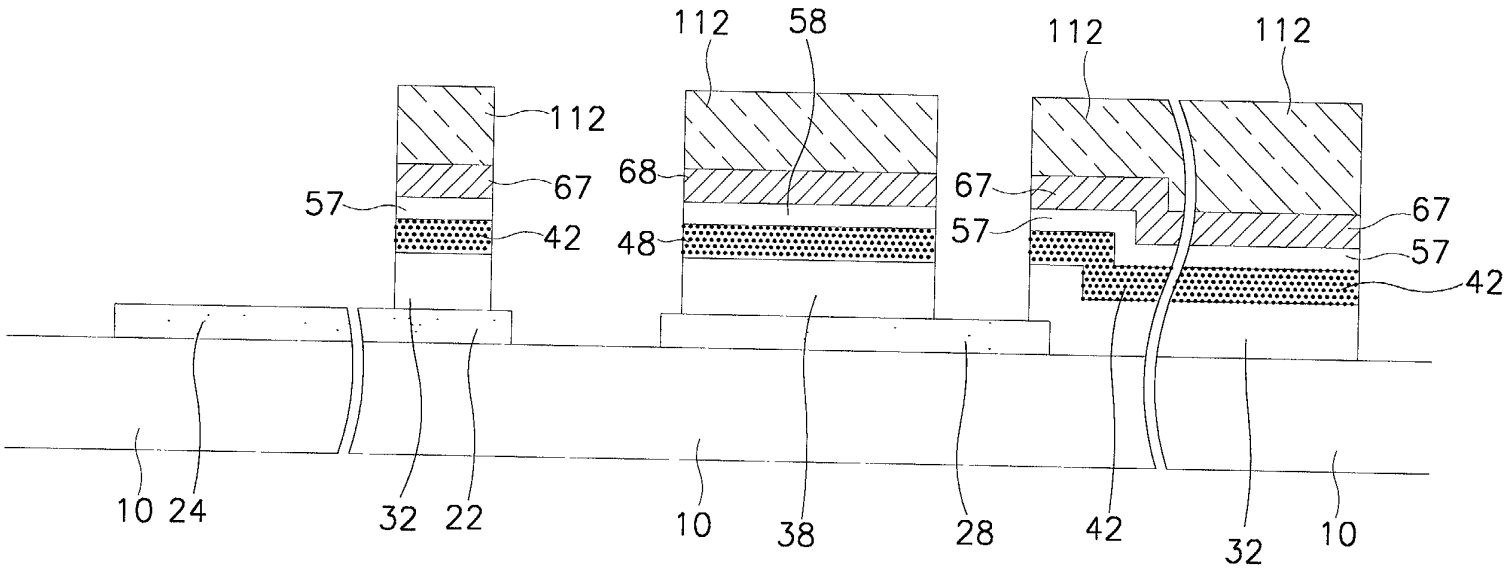
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FIG.11B

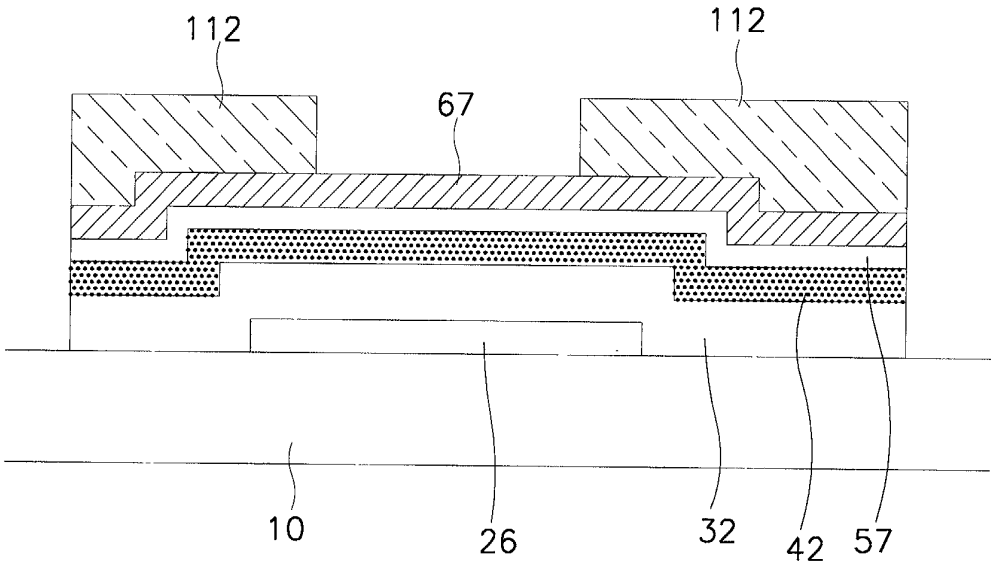

FIG. 12A

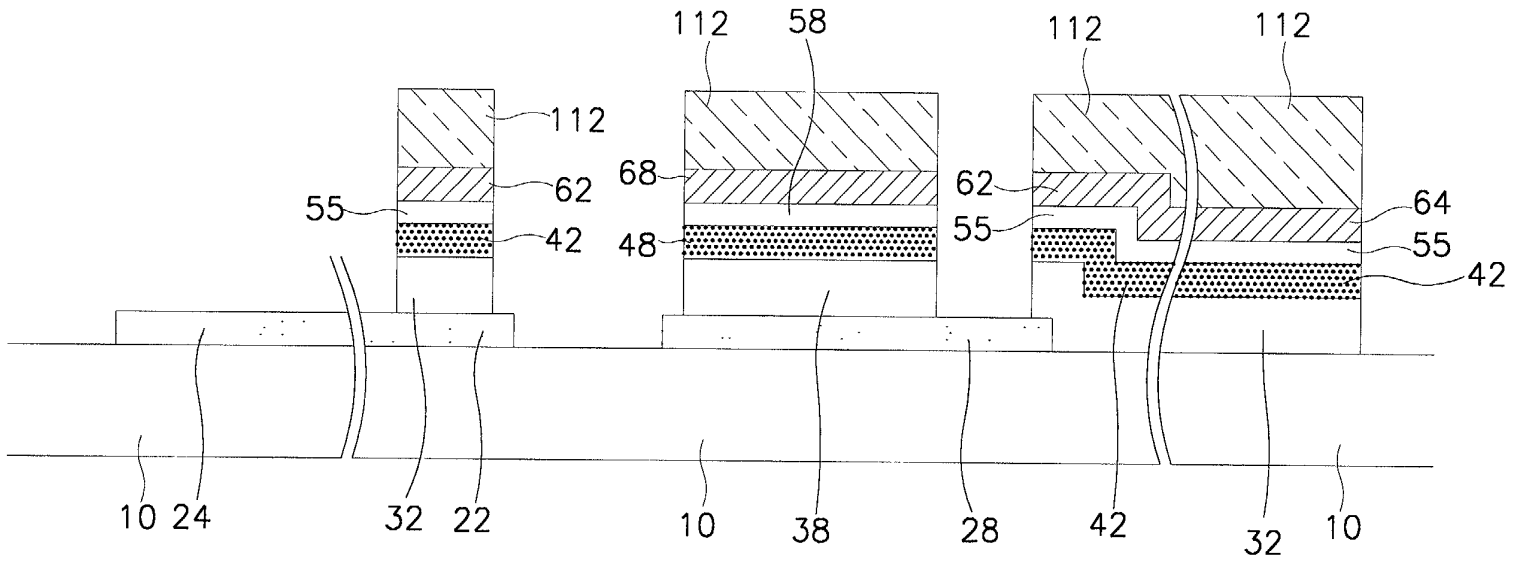

FIG.12B

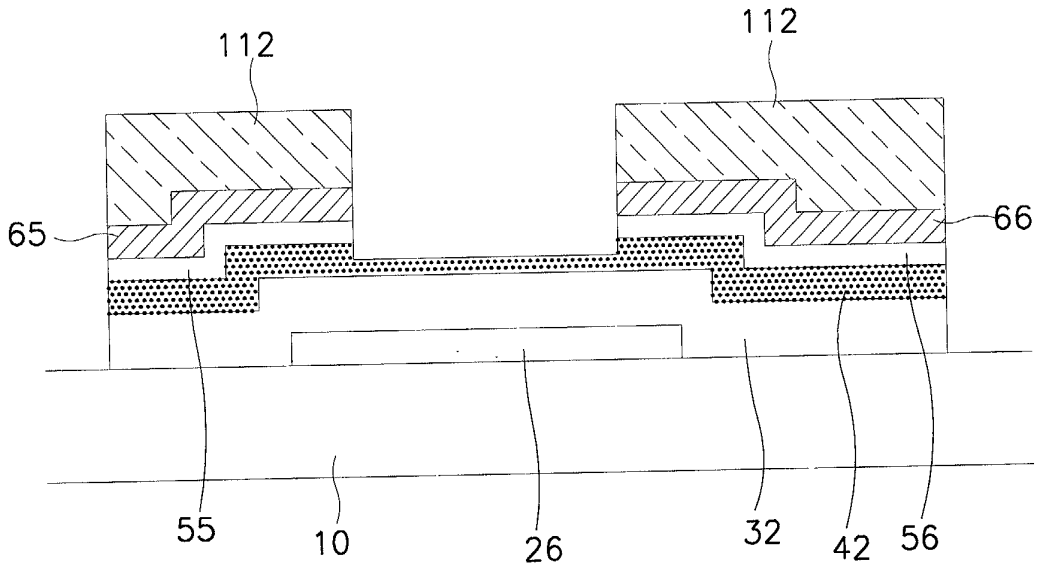

FIG. 13A

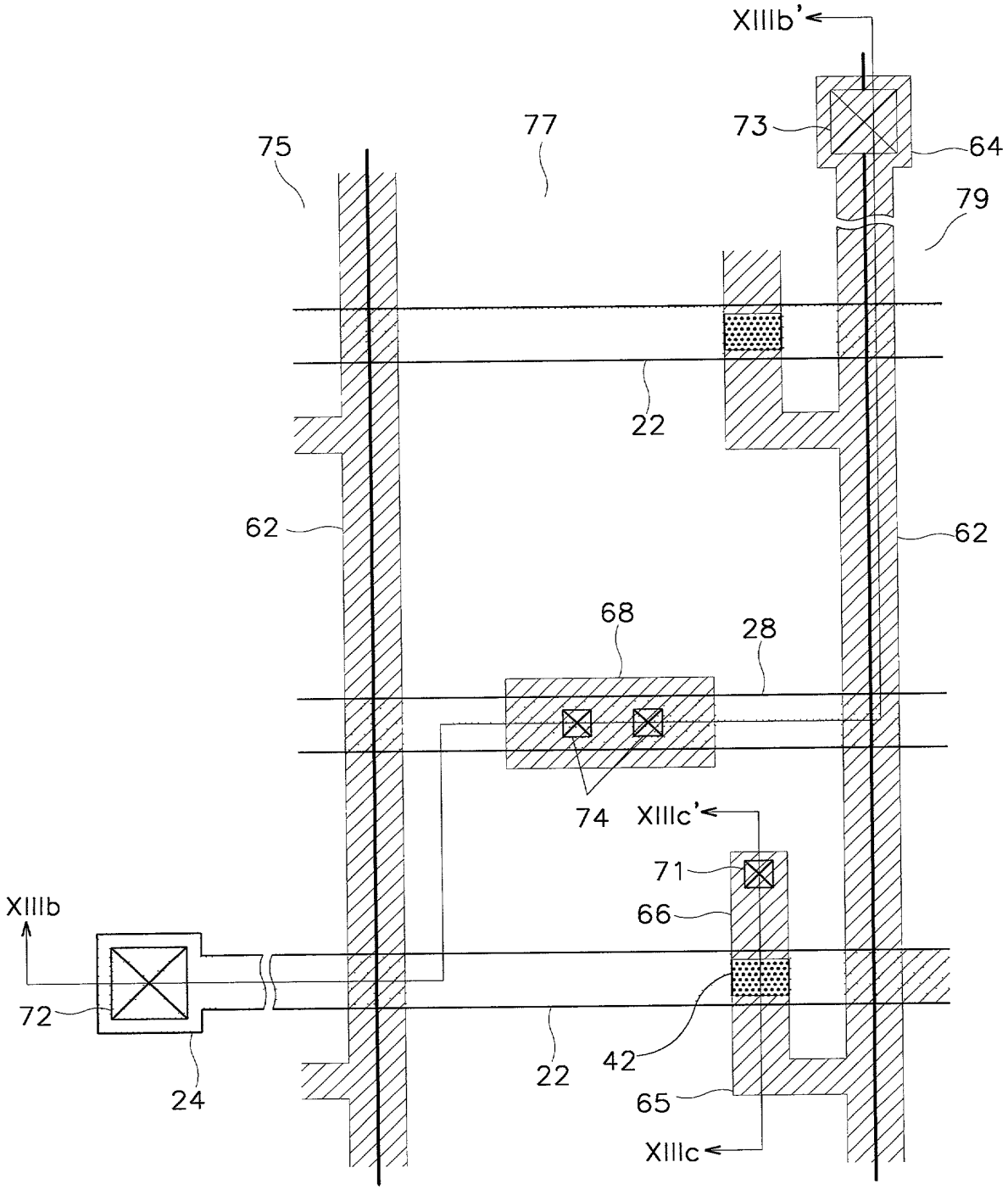
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FIG. 13B

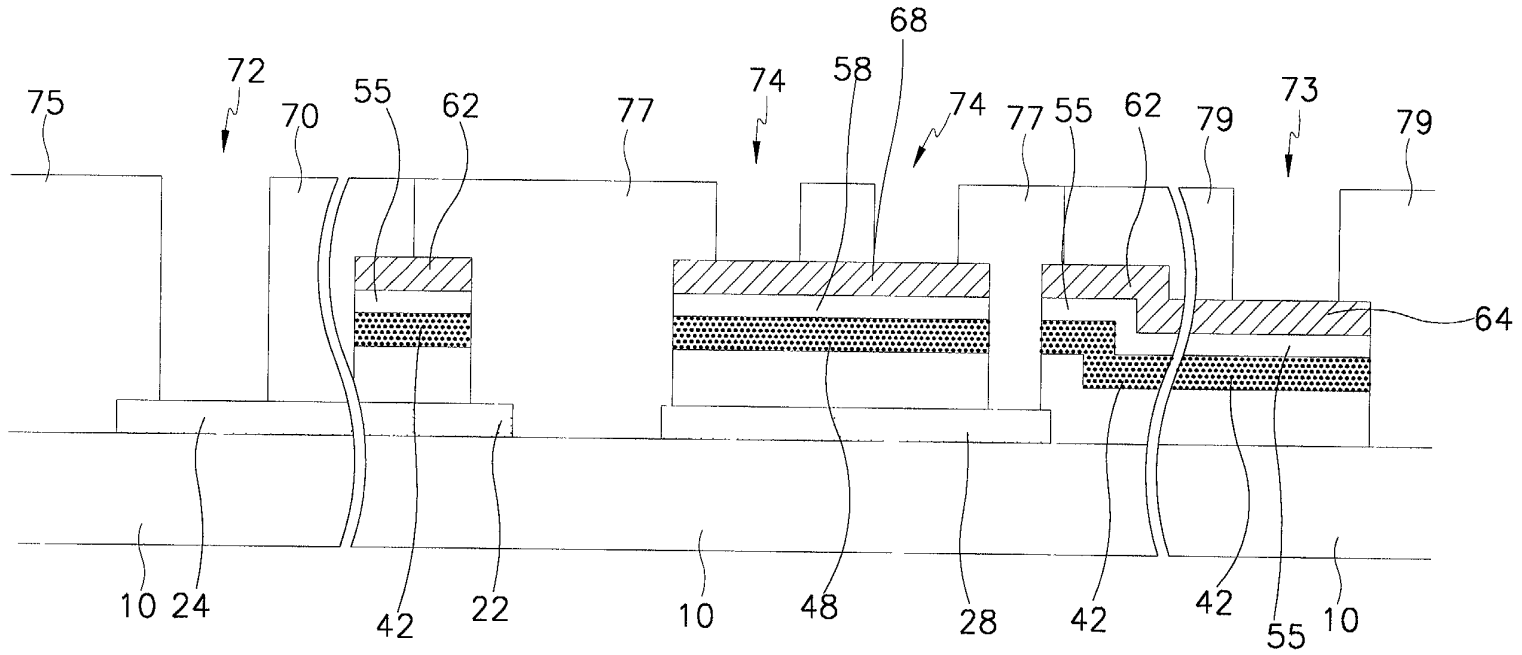
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FIG.13C

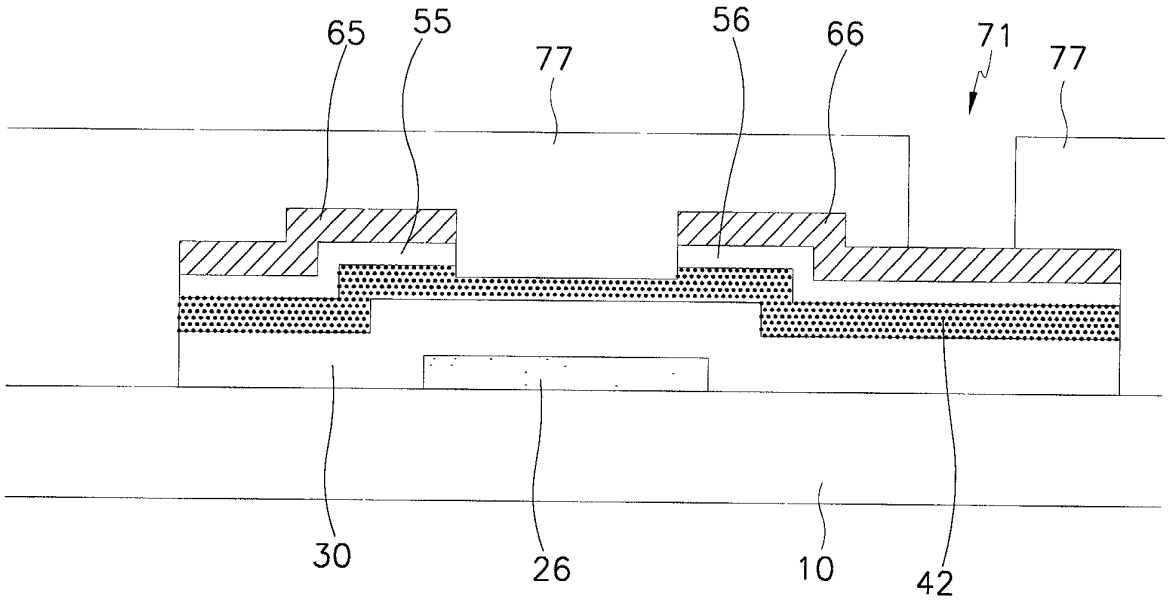

FIG. 14

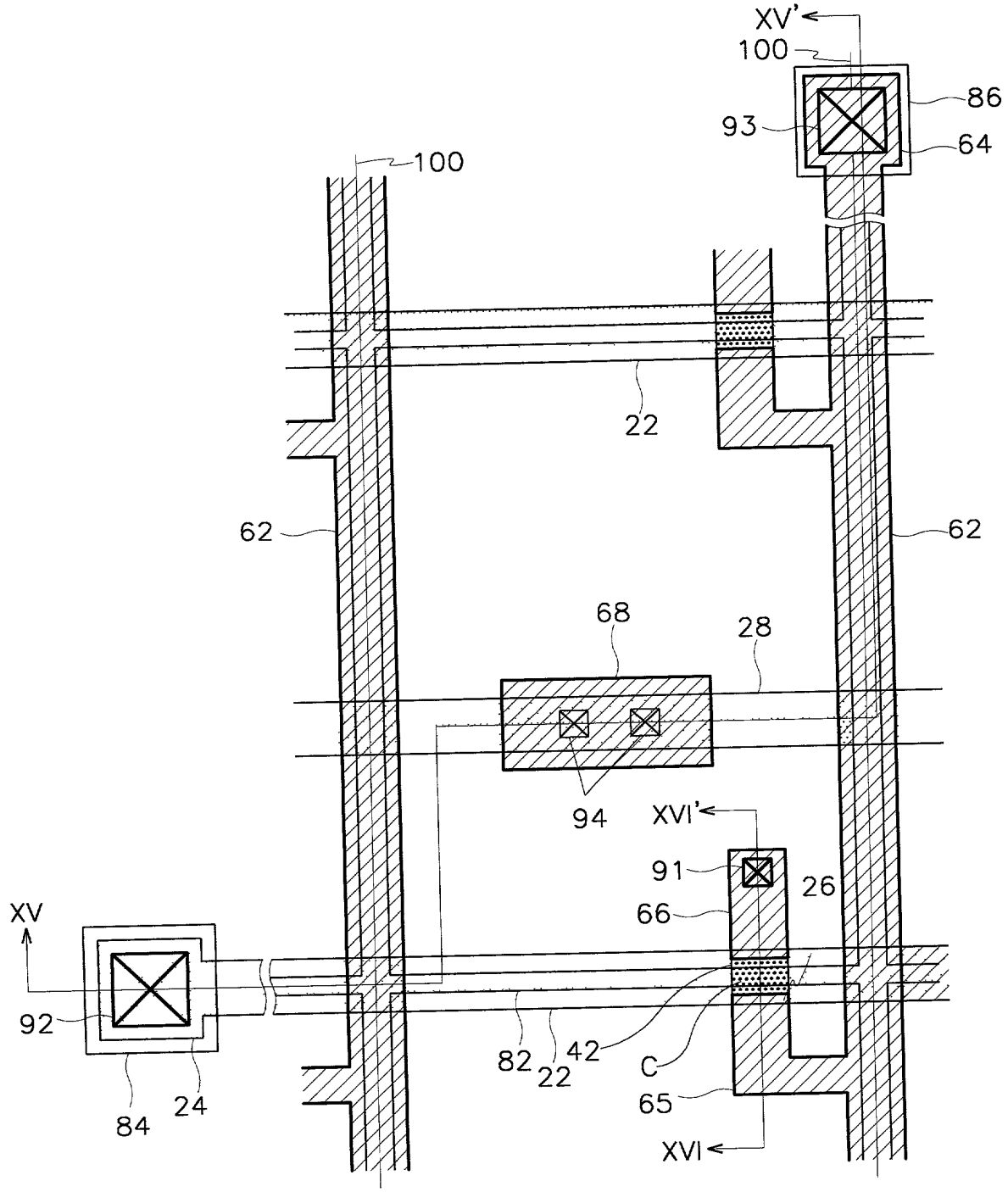
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FIG.15

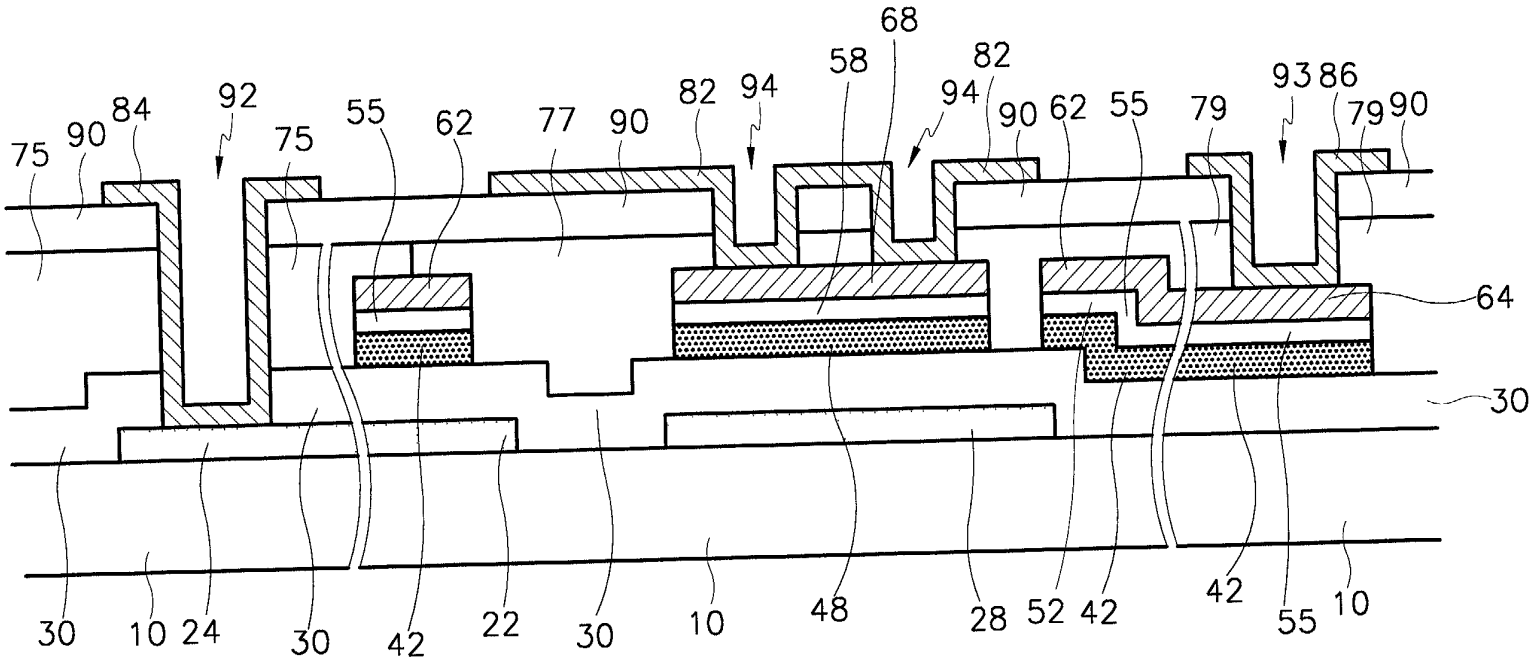
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FIG. 16

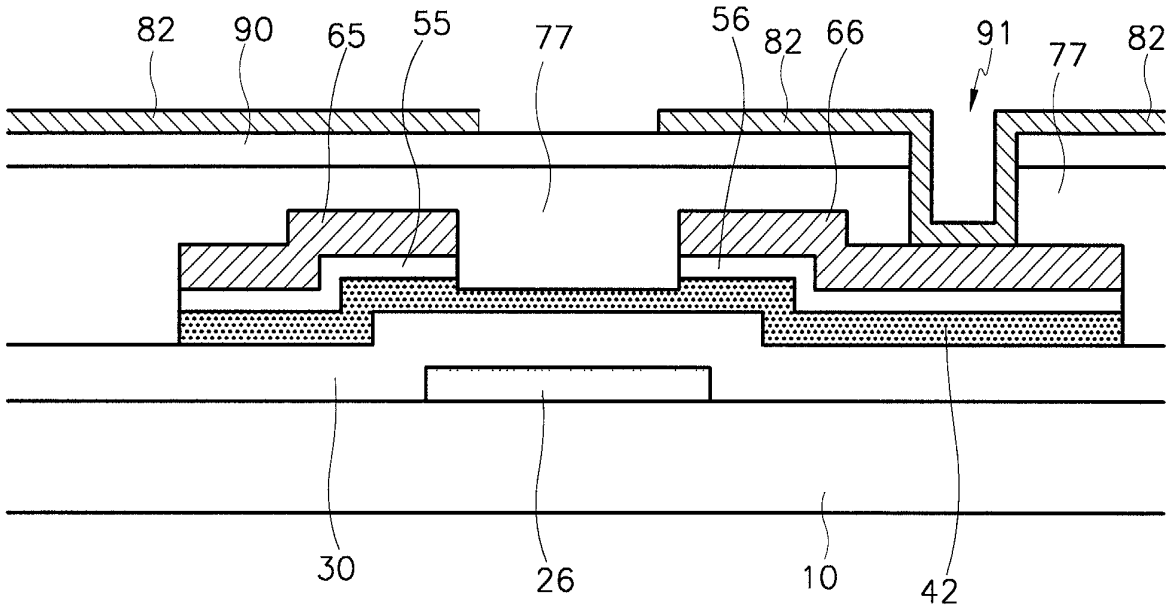


FIG.17A

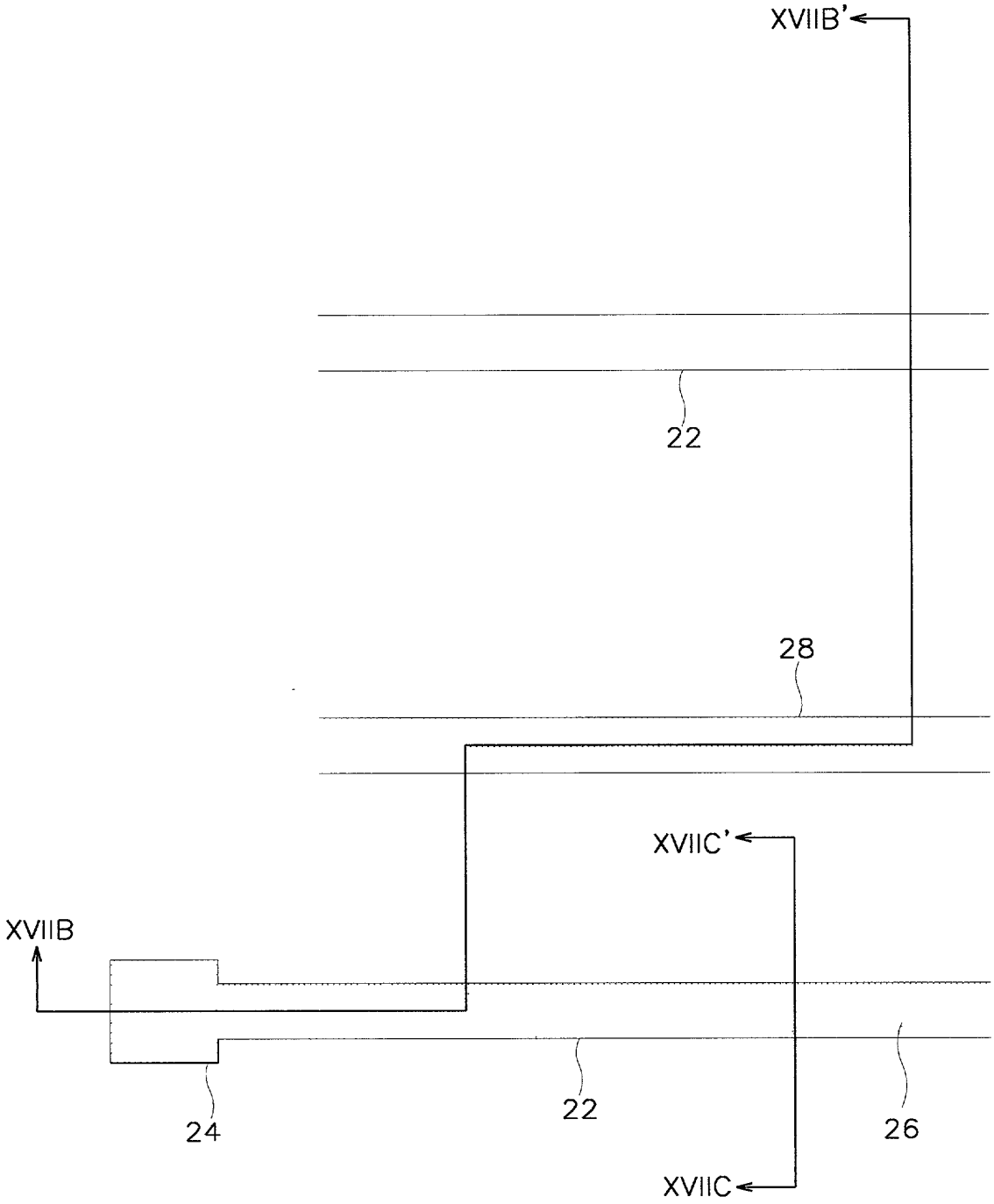


FIG.17B

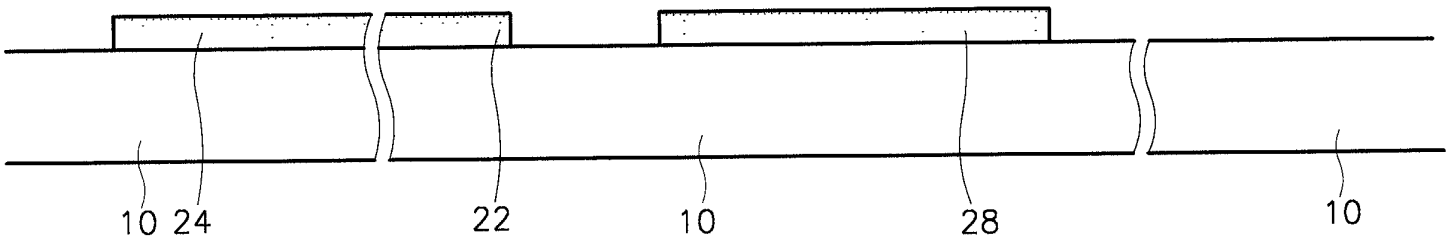


FIG.17C

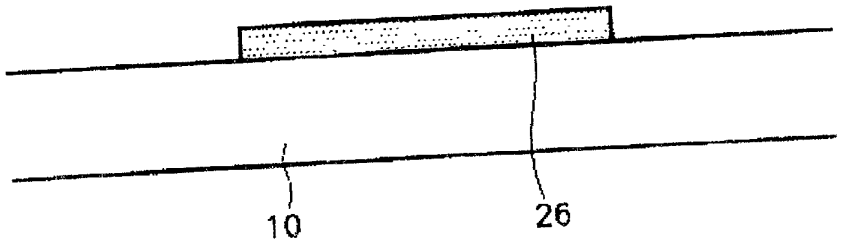


FIG.18A

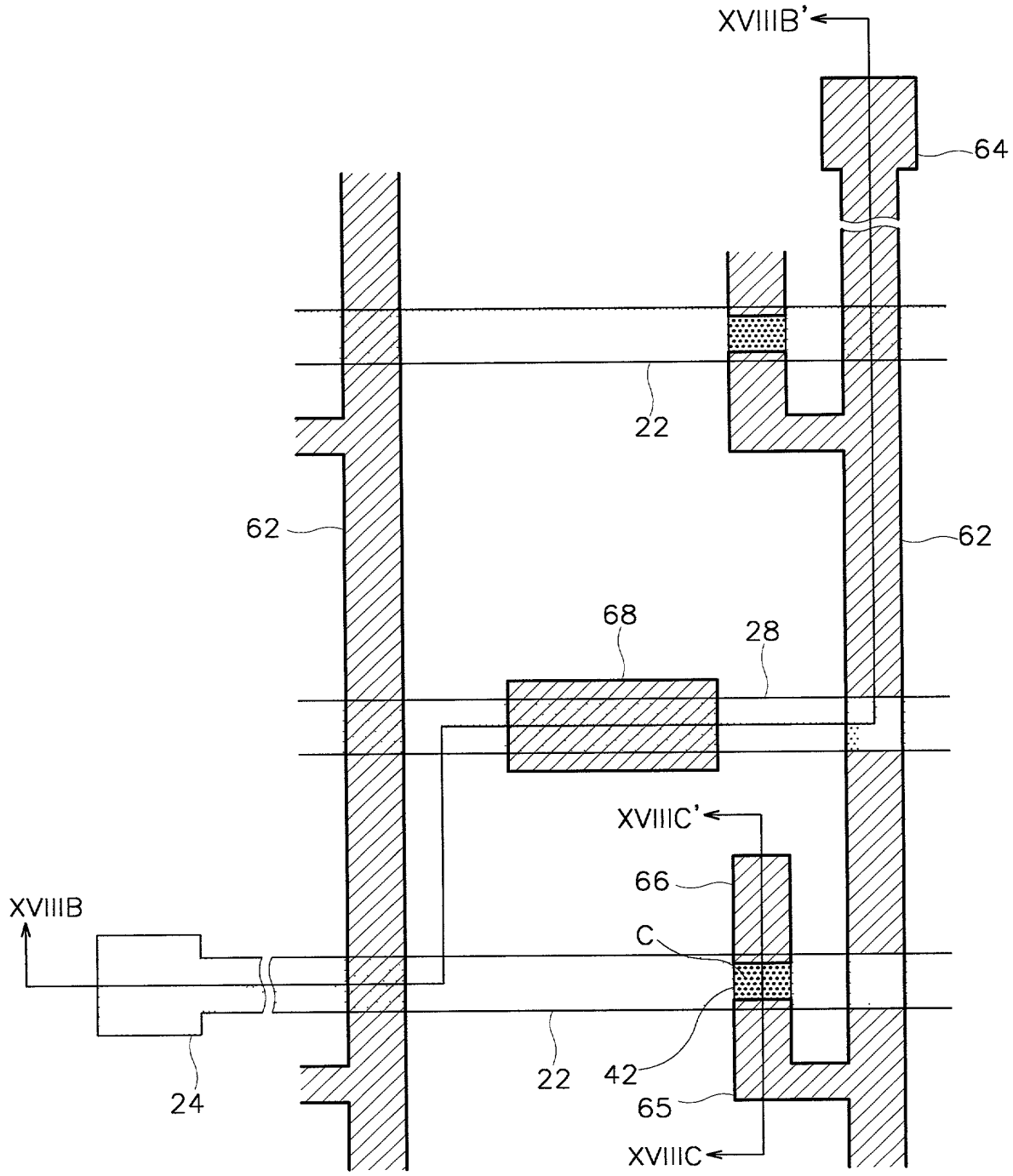


FIG.18B

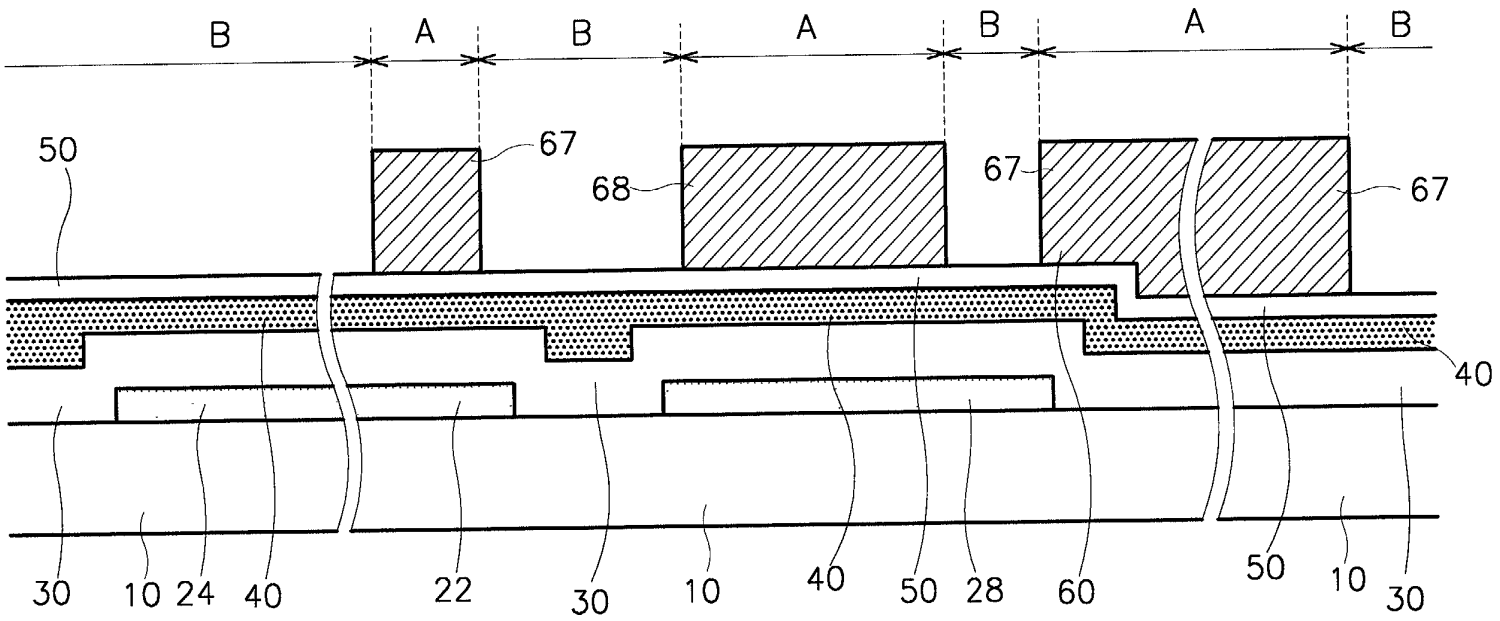


FIG.18C

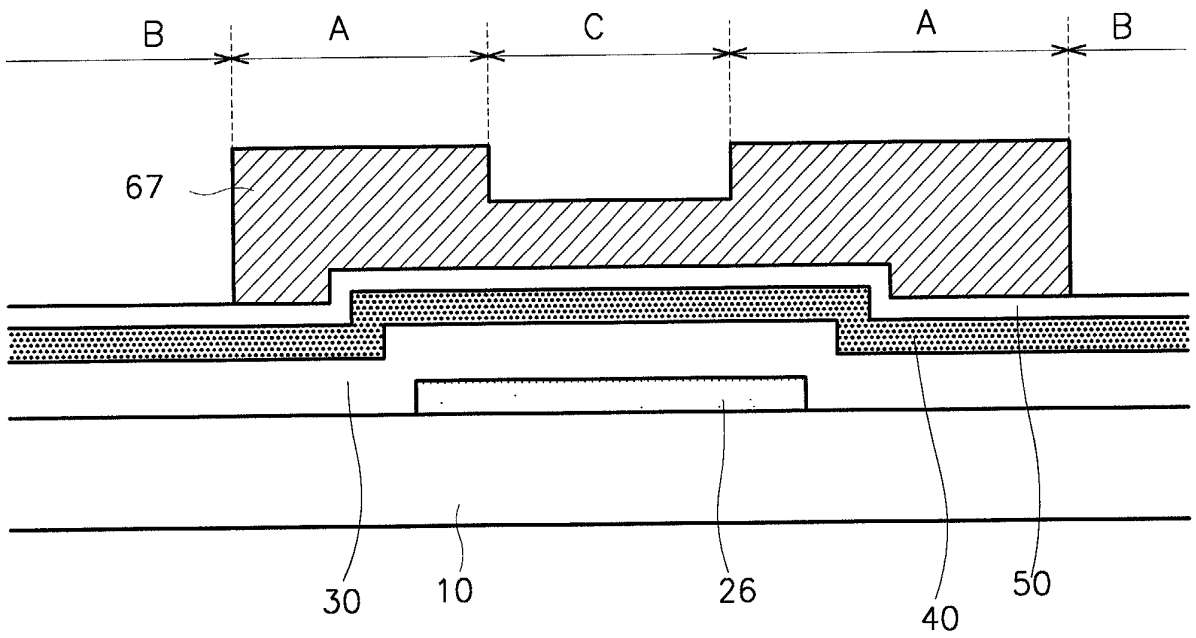


FIG.19A

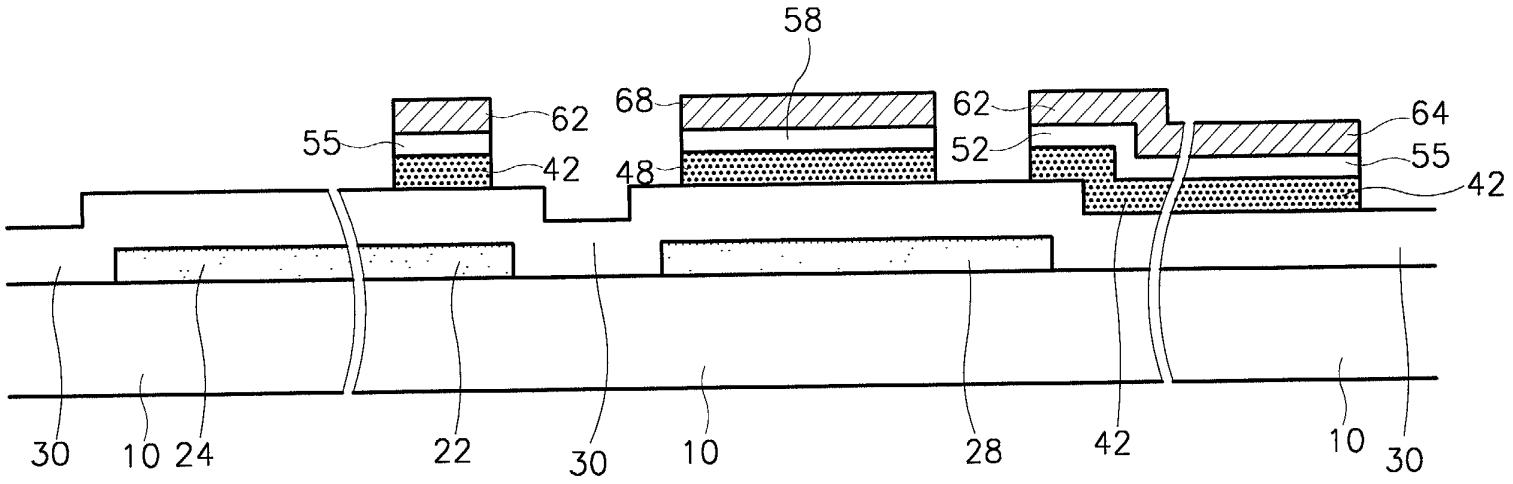


FIG.19B

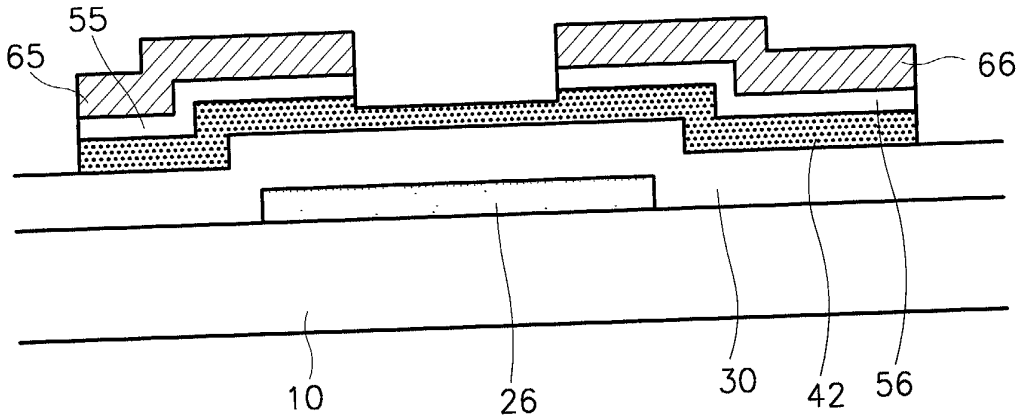


FIG.20A

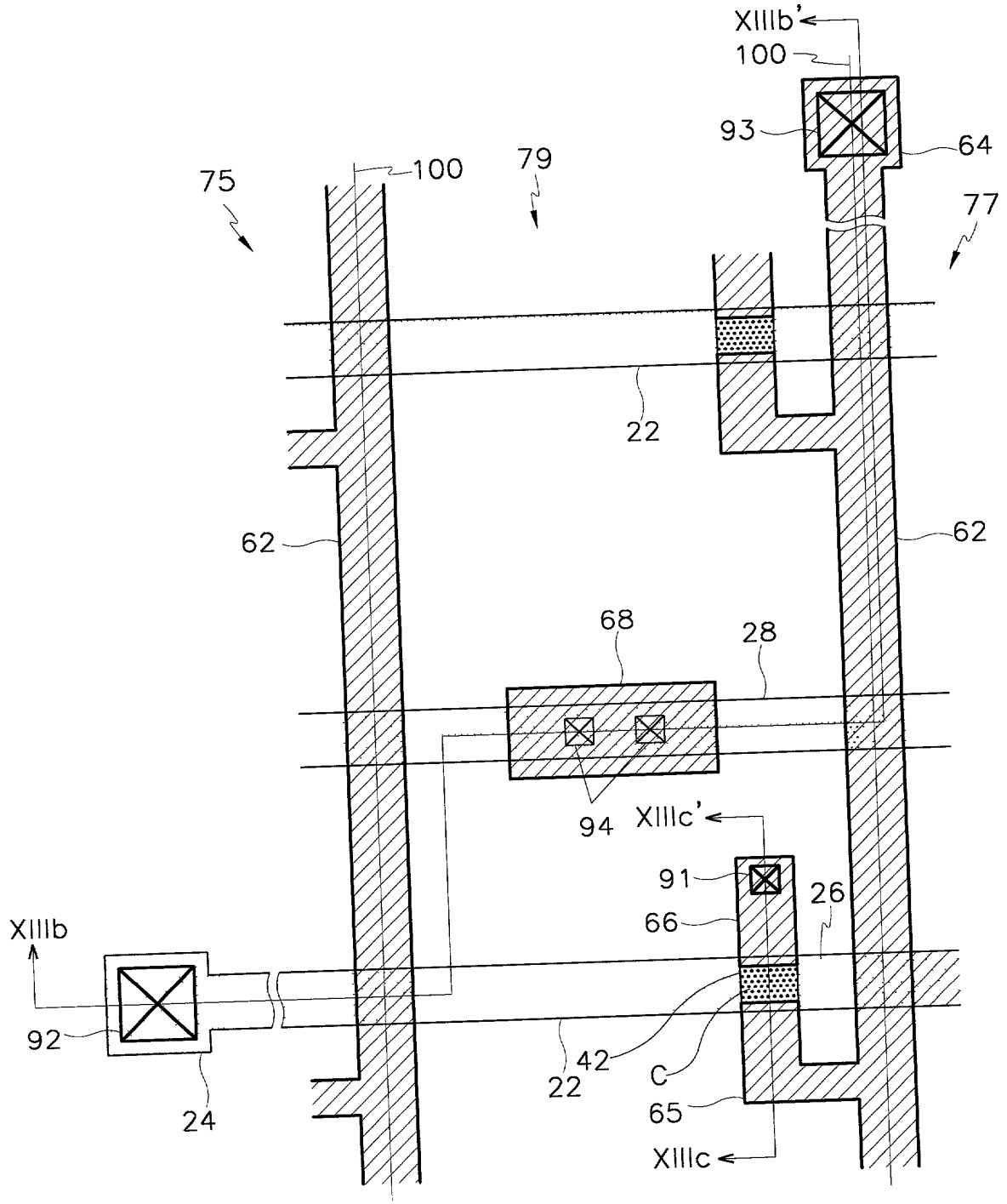

XIIIb'
100
93
64
75
100
79
77
22
62
62
68
28
94
XIIIc'
91
26
66
XIIIb
92
24
22
42
C
65
XIIIc

FIG.20B

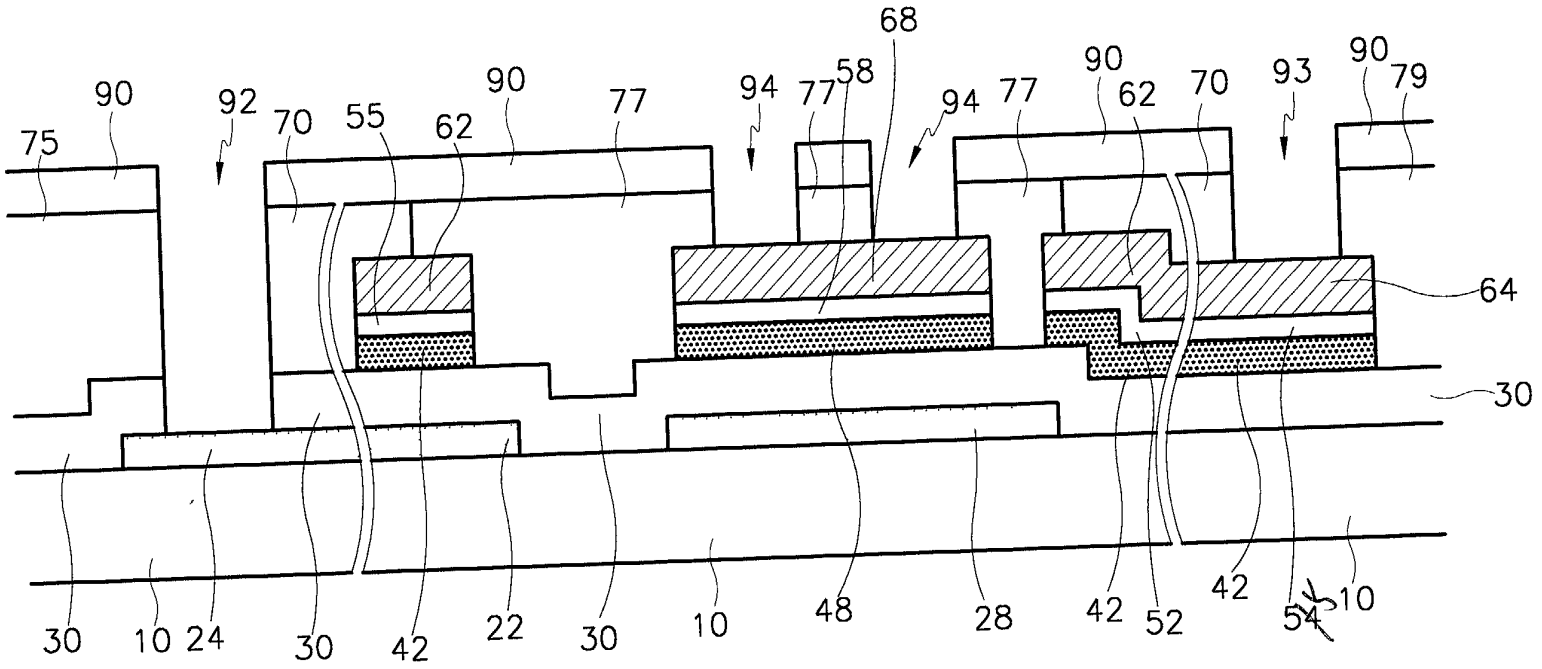


FIG.20C

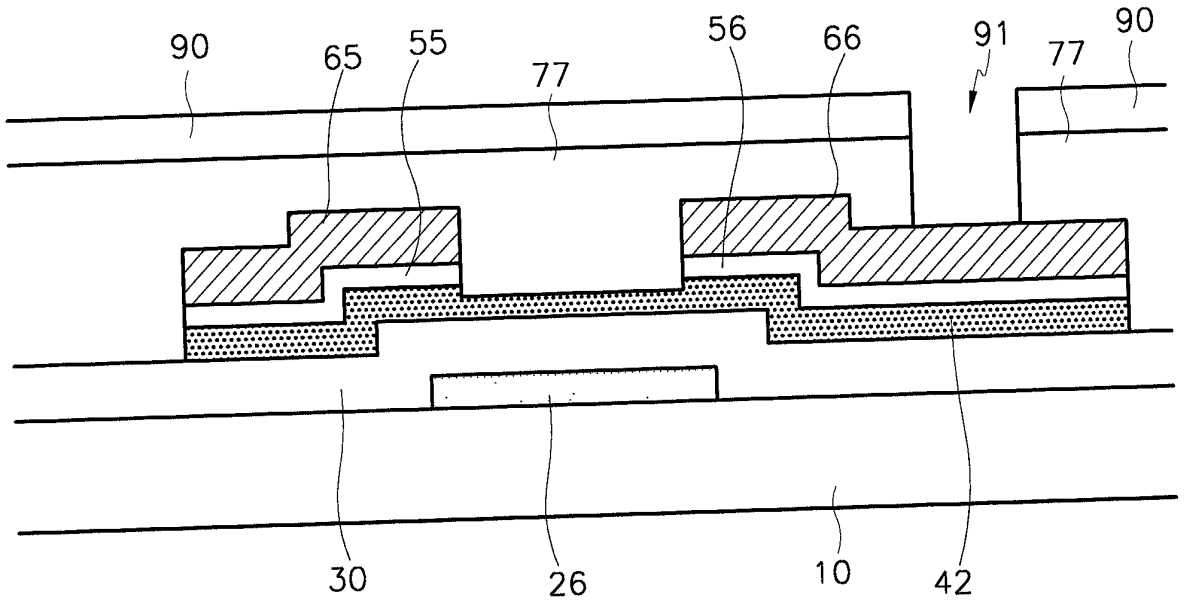


FIG.21

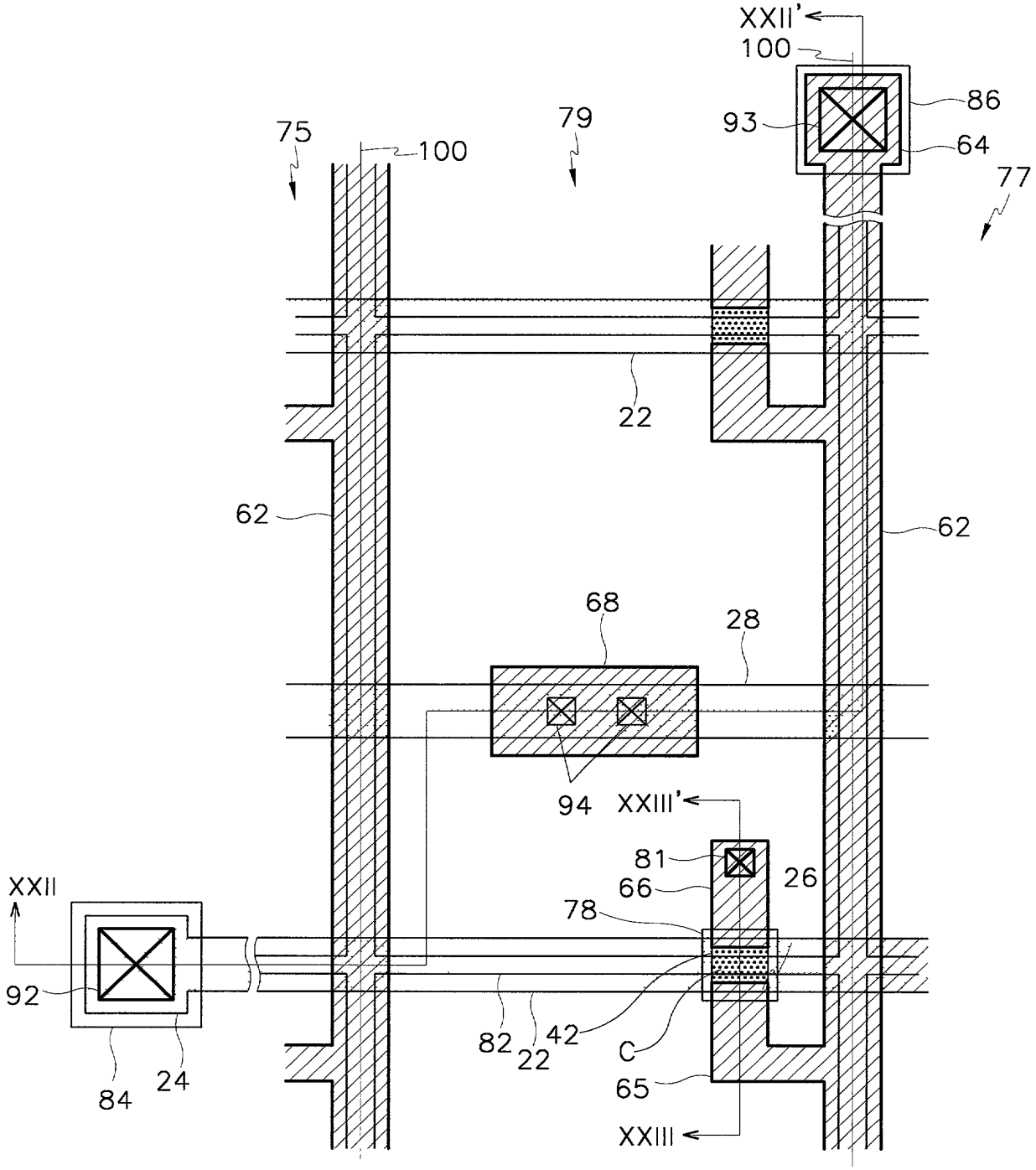

XXII'
100
86
93
64
77
75
100
79
22
62
62
68
28
94
XXIII'
81
66
26
78
XXII
92
84
24
82
22
42
C
65
XXIII

FIG.22

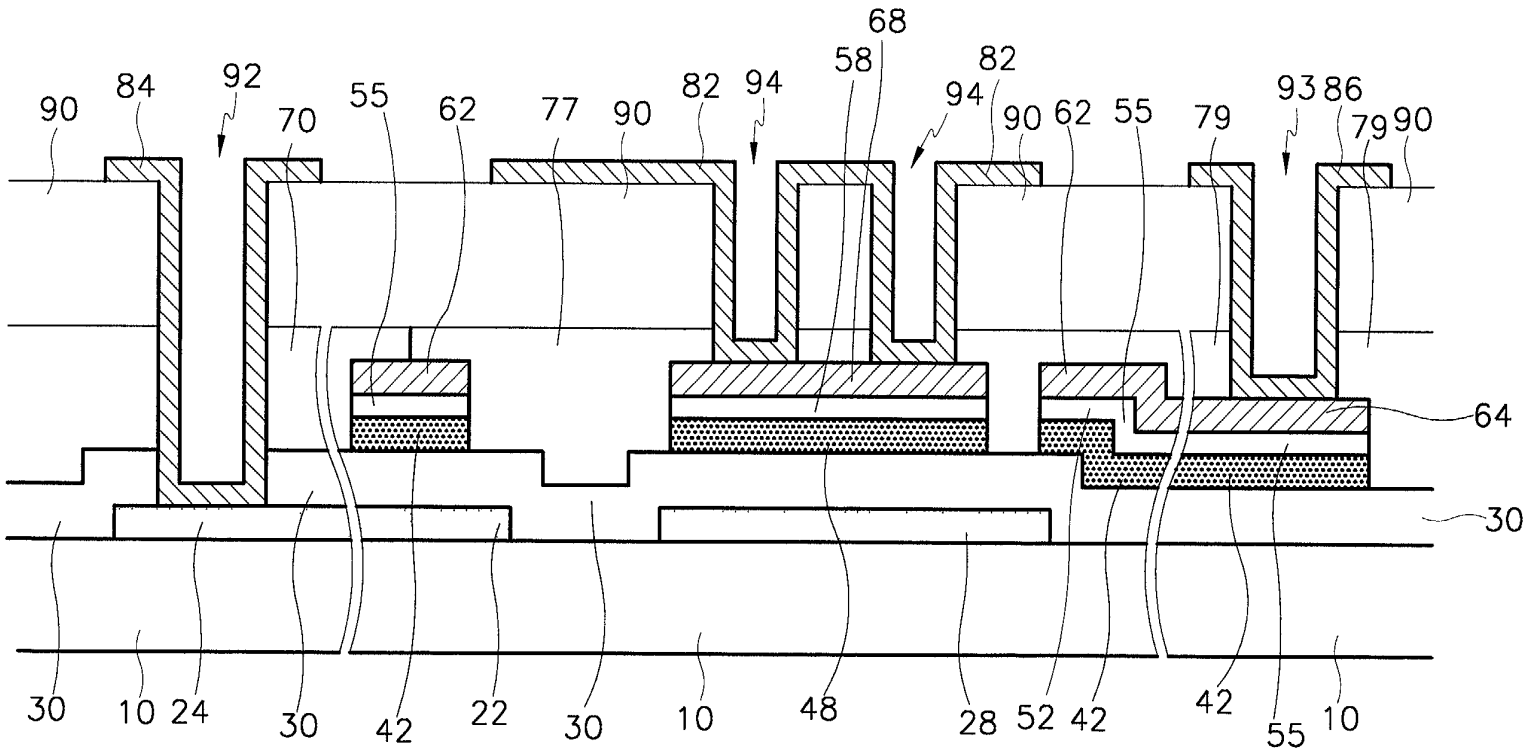
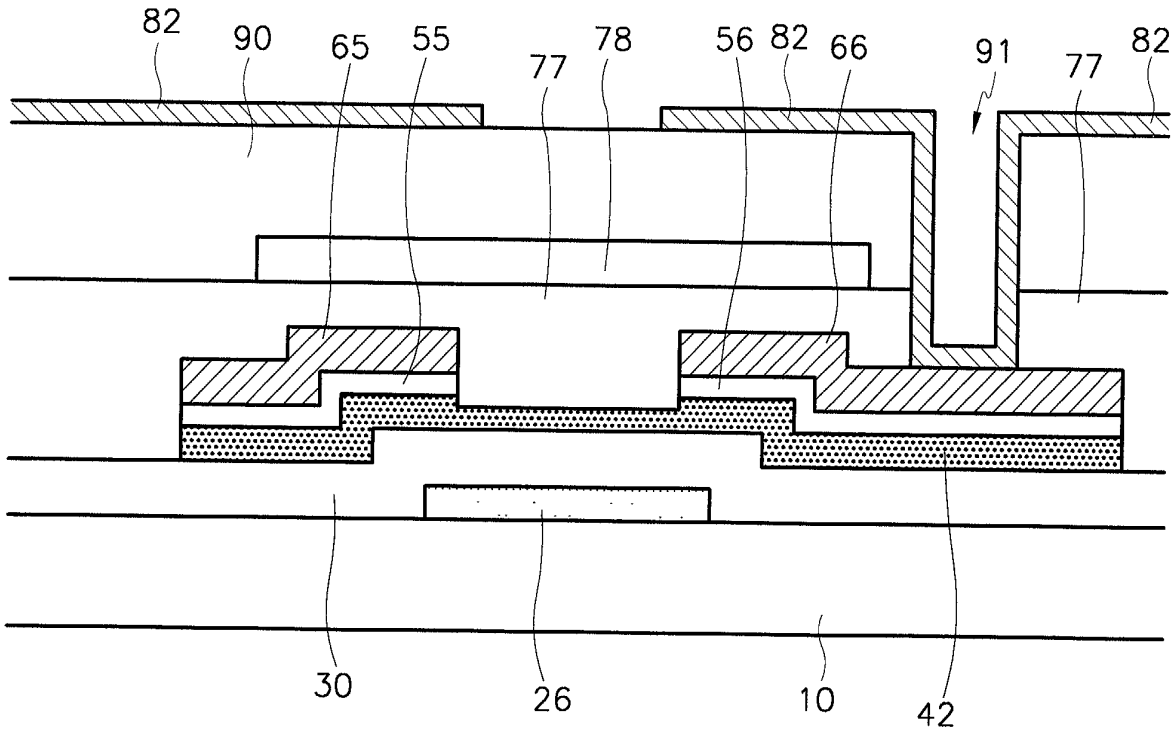


FIG.23



Combined Declaration and Power of Attorney for Patent Application

Docket Number:

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter that is claimed and for which a patent is sought on the invention entitled THIN FILM TRANSISTOR ARRAY PANELS AND METHODS FOR MANUFACTURING THE SAME, the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____;
as United States Application Number or PCT International Application Number _____; and
was amended on _____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information that is material to patentability as defined in 37 C.F.R. § 1.56.

I hereby claim foreign priority benefits under 35 U.S.C. § 119(a)-(d) or § 365(b) of any foreign application(s) for patent or inventor's certificate, or § 365(a) of any PCT international application, which designated at least one country other than the United States listed below, and have also identified below any foreign application for patent or inventor's certificate, or PCT international application having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)			Priority Claimed
			☒ Yes ☐ No
1999-14896 (Application No.)	KOREA (Country)	26/04/1999 (Day/Month/Year Filed)	
1999-14898 (Application No.)	KOREA (Country)	26/04/1999 (Day/Month/Year Filed)	
2000-19712 (Application No.)	KOREA (Country)	14/04/2000 (Day/Month/Year Filed)	

I hereby claim the benefit under 35 U.S.C. § 119(e) of any United States provisional application(s) listed below.

(Application No.)	(Filing Date)
(Application No.)	(Filing Date)

I hereby claim the benefit under 35 U.S.C. § 120 of any United States application(s), or under § 365(c) of any PCT international application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT international application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge

Appl. No. _____
Docket No.

the duty to disclose information that is material to patentability as defined in 37 C.F.R § 1.56 that became available between the filing date of the prior application and the national or PCT international filing date of this application.

(Application No.)	(Filing Date)	(Status - patented, pending, abandoned)

I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith:

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I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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Third inventor's signature		Date
Residence		
Citizenship		
Post Office Address		